

NOTES:  
1.HSF Property:Comply iSupplier system HSF property attribute up-to-date value.

2018.03.30

INVENTEC				
TITLE				
MODEL,PROJECT,FUNCTION				
SIZE A3	CODE CS	DOC NUMBER 1310A29944-0-0		REV X01

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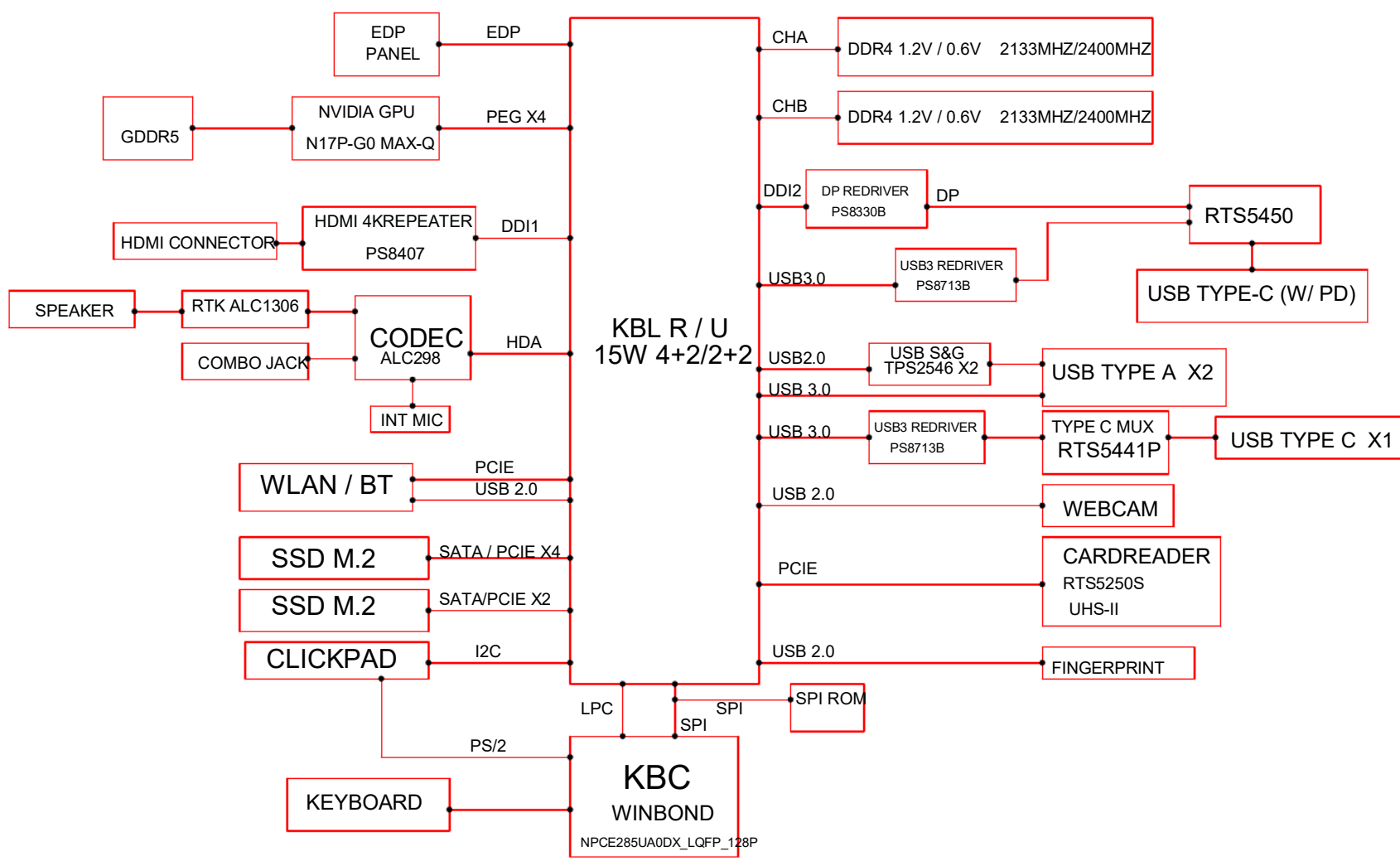
51 NGFF M.2 SSD2  
 52 DP REDRIVER  
 53 USB3 REDRIVER  
 54 TYPE C RTS5450  
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 69 DGPU\_CORE\_RT8816A  
 70 DGPU\_P1V5S  
 71 DGPU\_P1V0S  
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**INVENTEC**

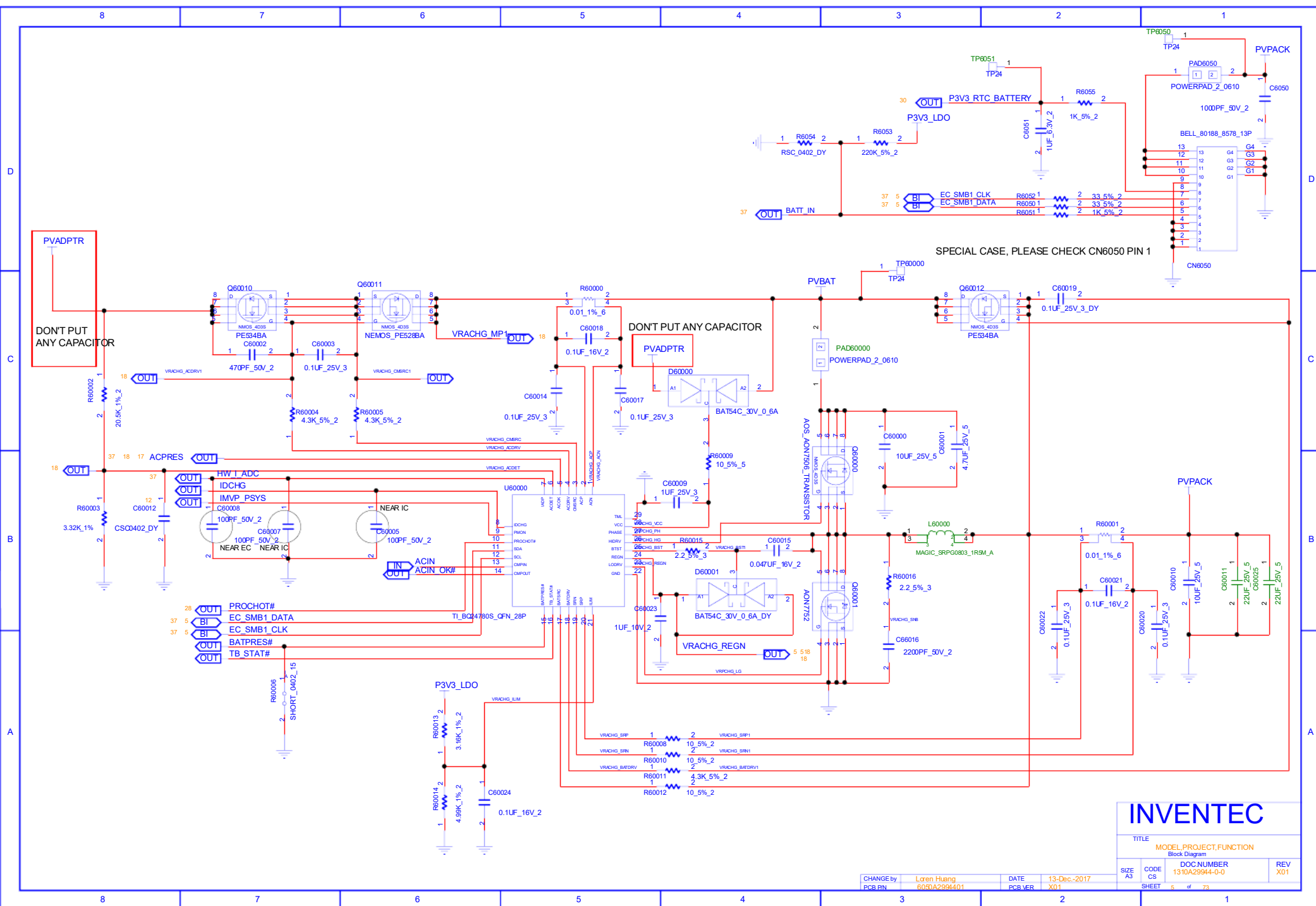
TITLE MODEL PROJECT FUNCTION  
INDEX

SIZE A3	CODE CS	DOC NUMBER 1310A29944-0-0	REV X01
SHEET		of 2 73	

CHANGE by PCB PIN	Loren Huang 88M02994401	DATE PCB VER	X03-Dec-2017
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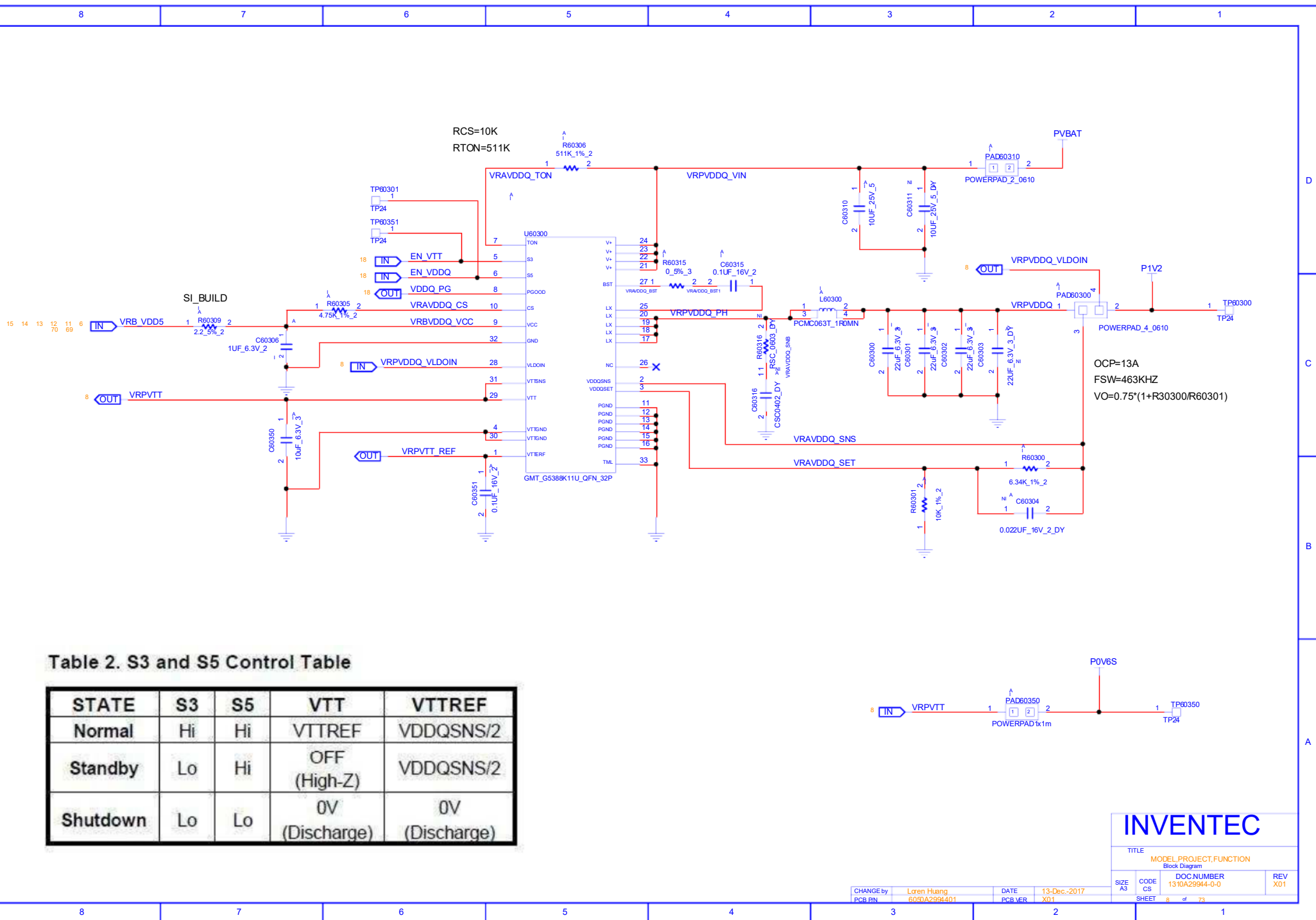












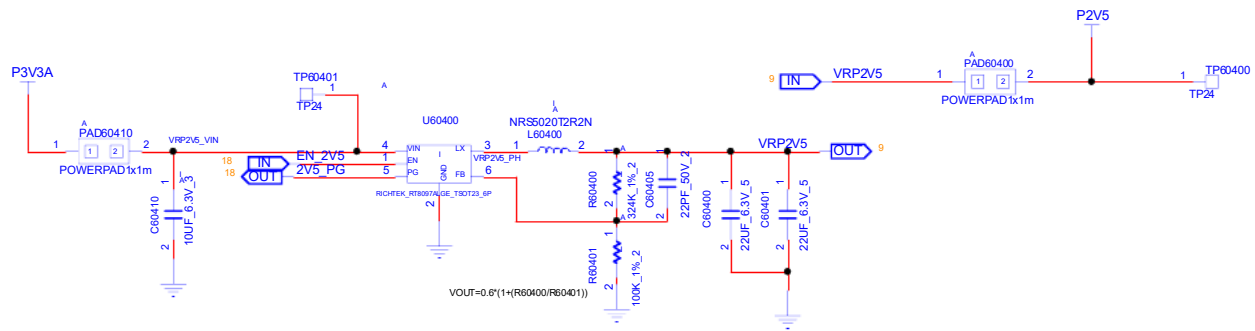
INVENTEC

TITLE  
MODEL PROJECT FUNCTION  
Block Diagram  
DOC NUMBER  
1310A29944-0-0  
REV  
X01

CHANGE by  
PCB BN  
Loren Huang  
6050A2994401  
DATE  
PCB VER  
13-Dec-2017  
X01

SHEET  
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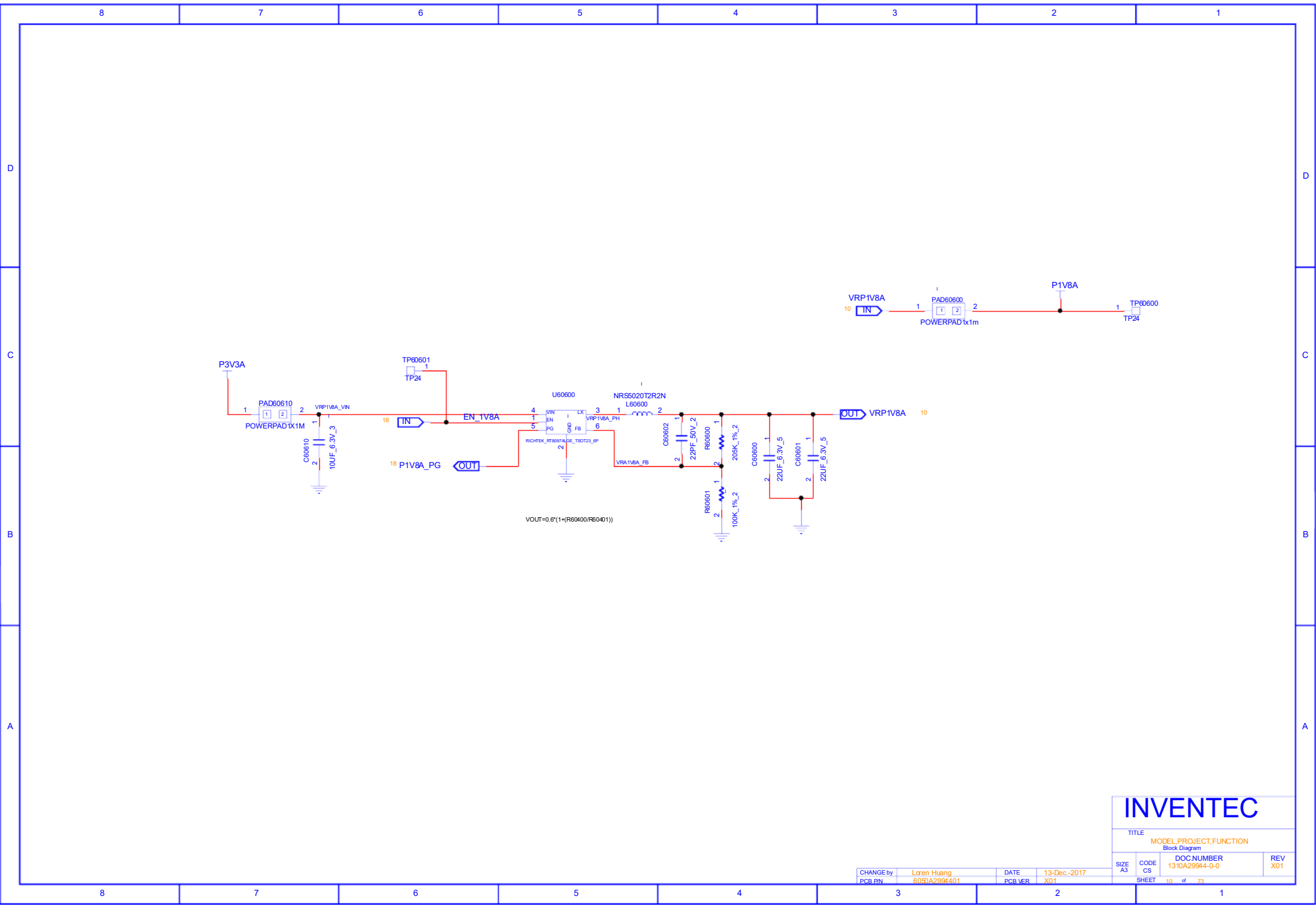




INVENTEC

TITLE			
MODEL PROJECT,FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310A29944-0-0	X01
SHEET 6 of 73			

CHANGE by	Loren Huang	DATE	13-Dec.-2017
PCB PIN	6050A2994401	PCB VER	X01

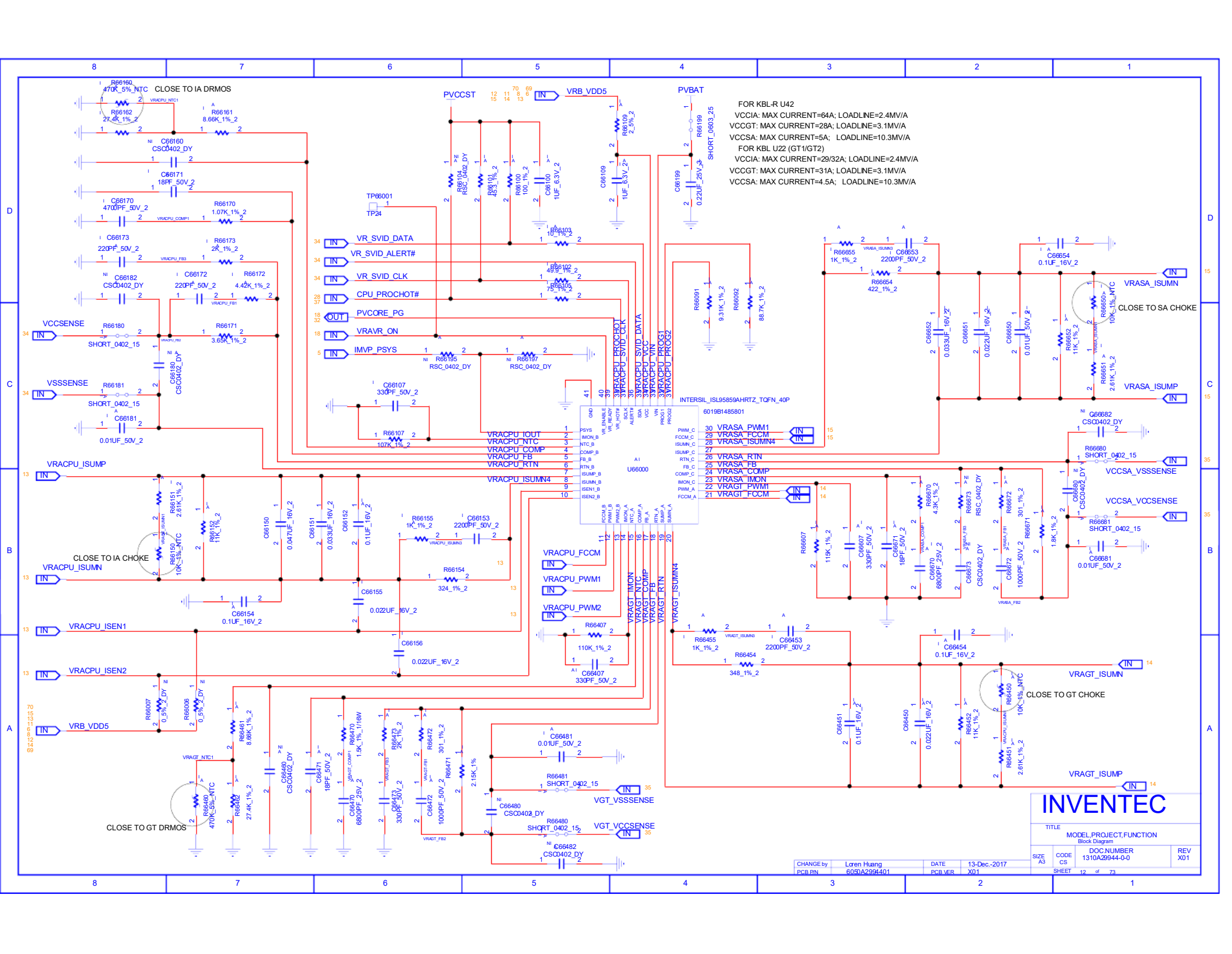


# INVENTEC

TITLE			
MODEL PROJECT FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310A29944-0-0	X01
SHEET	10	of	73

CHANGE by	Loren Huang	DATE	13-Dec-2017
PCB PIN	6050A2994401	PCB VER	X01





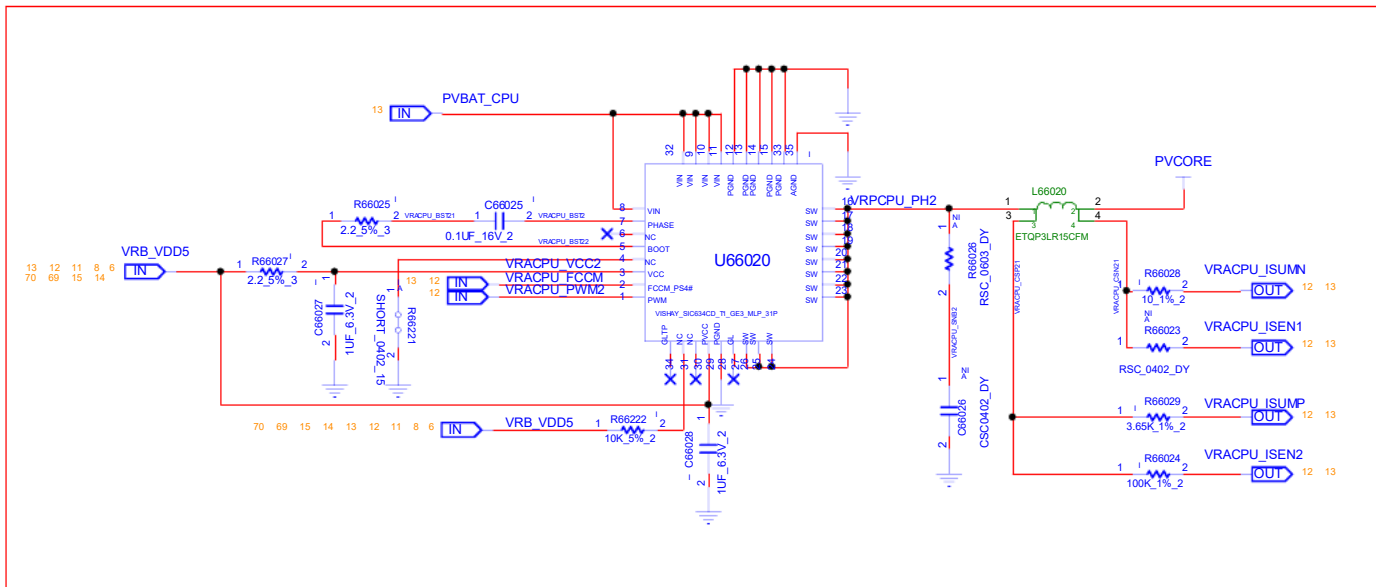
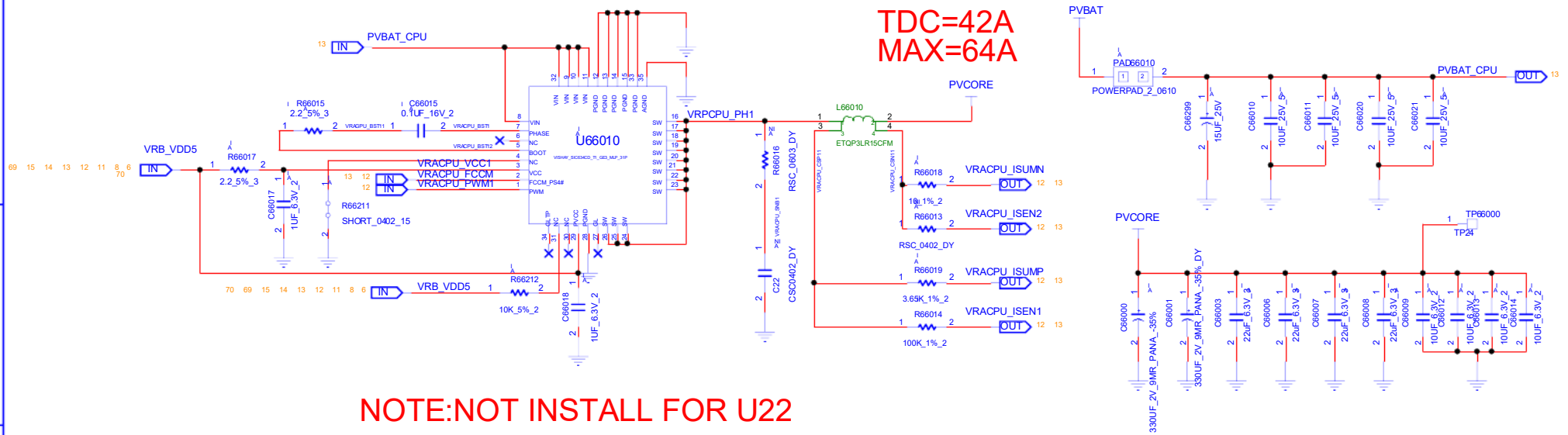
FOR KBL-R U42  
VCCIA: MAX CURRENT=64A; LOADLINE=2.4MV/A  
VCCGT: MAX CURRENT=28A; LOADLINE=3.1MV/A  
VCCSA: MAX CURRENT=5A; LOADLINE=10.3MV/A  
FOR KBL U22 (GT1/GT2)  
VCCIA: MAX CURRENT=29/32A; LOADLINE=2.4MV/A  
VCCGT: MAX CURRENT=31A; LOADLINE=3.1MV/A  
VCCSA: MAX CURRENT=4.5A; LOADLINE=10.3MV/A

INVENTEC			
MODEL PROJECT:FUNCTION			
Block Diagram			
SIZE A3		DOC NUMBER	
CODE CS		1310A29944-0-0	
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REV X01			

CHANGE by	Loren Huang	DATE	13-Dec.-2017
PCB PIN	6050A29944-01	PCB VER	X01

NOTE:ONE PHASE FOR U22

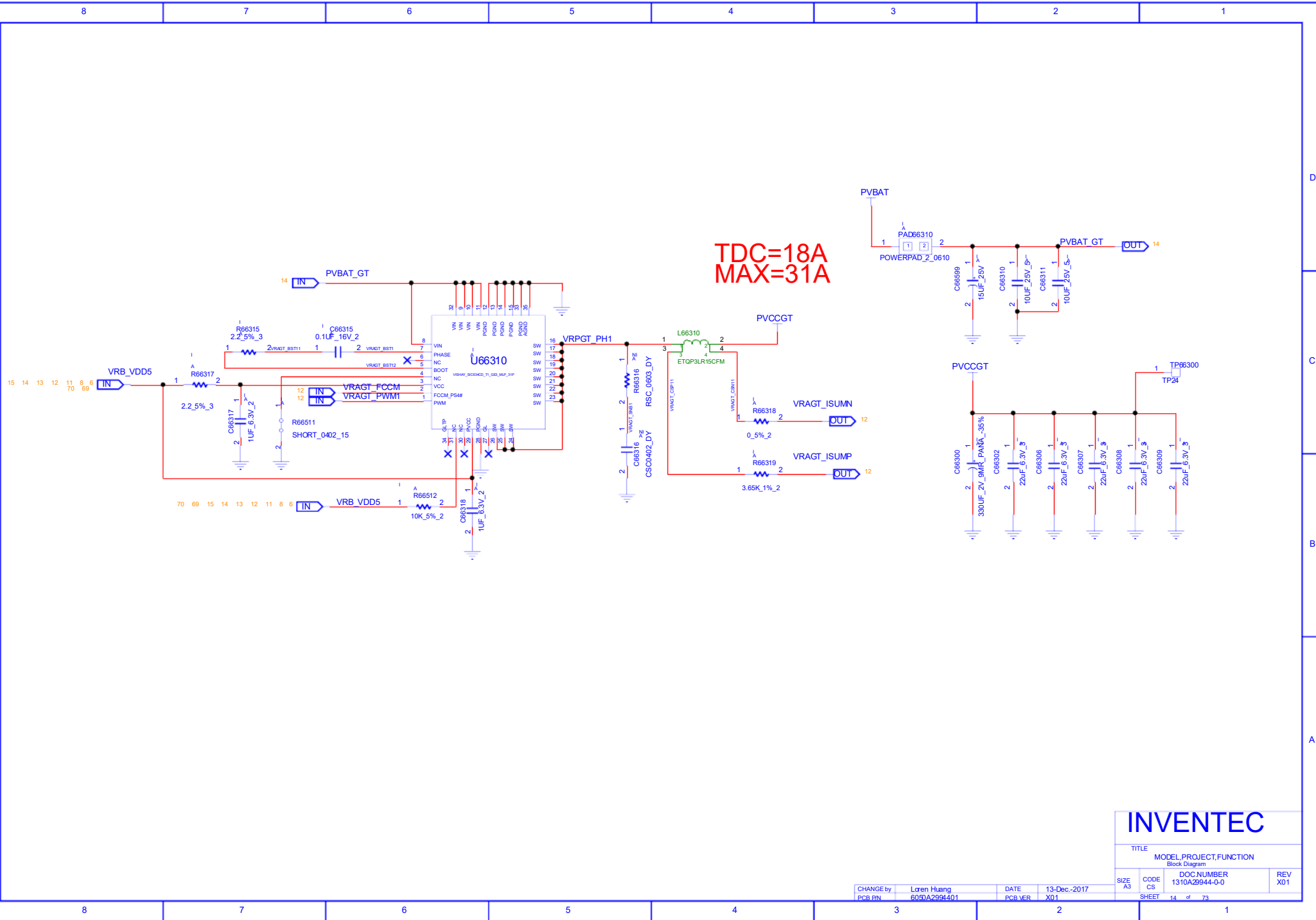
TDC=42A  
MAX=64A



INVENTEC

TITLE			
MODEL PROJECT:FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310A29944-0-0	X01
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CHANGE by	Loren Huang	DATE	13-Dec.-2017
PCB RN	6050A2994401	PCB VER	X01



TDC=18A  
MAX=31A

INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310A29944-0-0	REV X01
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CHANGE by	Loren Huang	DATE	13-Dec.-2017
PCB.DN	6050A2994401	PCB.VER	X01



U42			U22		
Location	IEC P/N	Description	Location	IEC P/N	Description
C66150	6010B0046101	CAP-CHIP,0.047UF,16V,K,X7R,0402,TAP	C66150	6010A0000101	CAP-CHIP-223-K,16V-X7R-0402-TAP
C66151	6010B0010101	CHIP,0.033UF,16V,K,X7R,0402,TR	C66151	6010B0010101_DY	CHIP,0.033UF,16V,K,X7R,0402,TR
R66006	60130B0000ZT_DY	RES-CHIP-00HM-5%-1/16W-0402-TAP	R66006	60130B0000ZT	RES-CHIP-00HM-5%-1/16W-0402-TAP
R66007	60130B0000ZT_DY	RES-CHIP-00HM-5%-1/16W-0402-TAP	R66007	60130B0000ZT	RES-CHIP-00HM-5%-1/16W-0402-TAP
C66155	6010A0000101	CAP-CHIP-223-K,16V-X7R-0402-TAP	C66155	6010A0000101_DY	CAP-CHIP-223-K,16V-X7R-0402-TAP
C66156	6010A0000101	CAP-CHIP-223-K,16V-X7R-0402-TAP	C66156	6010A0000101_DY	CAP-CHIP-223-K,16V-X7R-0402-TAP
R66154	6013A008780S	RES-CHIP-383-1%-1/16W-0402-TAP	R66154	6013A008780D	RES-CHIP-287-1%-1/16W-0402-TAP
R66171	6013A0088207	RES-CHIP-3.65K-1%-1/16-0402-TAP	R66171	6013B0097601	RES-CHIP,1.69K,1%,1/16W,0402,TAP
R66107	6013A0088708	RES-CHIP-107K-1%-1/16-0402-TAP	R66107	6013A0014701	RES-CHIP-100K-1%-1/16W-0402-TAP
C66020	6010B0150801	CHIP,10UF,25V,K,X5R,0805,TR,1.25MM	C66020	6010B0150801_DY	CHIP,10UF,25V,K,X5R,0805,TR,1.25MM
C66021	6010B0150801	CHIP,10UF,25V,K,X5R,0805,TR,1.25MM	C66021	6010B0150801_DY	CHIP,10UF,25V,K,X5R,0805,TR,1.25MM
R66014	6013A0014701	RES-CHIP-100K-1%-1/16W-0402-TAP	R66014	6013A0014701_DY	RES-CHIP-100K-1%-1/16W-0402-TAP
U66020	6019B1530201	IC,MOSFET DRIVER,40A,MLP55-31L,31P,TR	U66020	6019B1530201_DY	IC,MOSFET DRIVER,40A,MLP55-31L,31P,TR
L66020	6014B0341701	INDUCTOR,0.15UH,+/- 20%,1MHZ,29A,7.3X8.7X3MM,SMD,TR	L66020	6014B0341701_DY	INDUCTOR,0.15UH,+/- 20%,1MHZ,29A,7.3X8.7X3MM,SMD,TR
R66025	60130B2R200T	RES-CHIP-2.2-5%-1/10W-0803-TAP	R66025	60130B2R200T_DY	RES-CHIP-2.2-5%-1/10W-0803-TAP
C66025	6010A0036403	CHIP,0.1UF,16V,K,X7R,0402,TAP	C66025	6010A0036403_DY	CHIP,0.1UF,16V,K,X7R,0402,TAP
R66027	60130B2R200T	RES-CHIP-2.2-5%-1/10W-0803-TAP	R66027	60130B2R200T_DY	RES-CHIP-2.2-5%-1/10W-0803-TAP
C66027	6010B0392101	CAPACITOR-CHIP,1UF,6.3V,K,X5R,0402,TR	C66027	6010B0392101_DY	CAPACITOR-CHIP,1UF,6.3V,K,X5R,0402,TR
C66028	6010B0392101	CAPACITOR-CHIP,1UF,6.3V,K,X5R,0402,TR	C66028	6010B0392101_DY	CAPACITOR-CHIP,1UF,6.3V,K,X5R,0402,TR
R66024	6013A0014701	RES-CHIP-100K-1%-1/16W-0402-TAP	R66024	6013A0014701_DY	RES-CHIP-100K-1%-1/16W-0402-TAP
R66028	6013A0014201	RES-CHIP-100HM-1%-1/16W-0402-TAP	R66028	6013A0014201_DY	RES-CHIP-100HM-1%-1/16W-0402-TAP
R66029	6013A0088207	RES-CHIP-3.65K-1%-1/16-0402-TAP	R66029	6013A0088207_DY	RES-CHIP-3.65K-1%-1/16-0402-TAP
R66222	60130B1030ZT	CHIP,10K,5%,1/16W,0402,TR	R66222	60130B1030ZT_DY	CHIP,10K,5%,1/16W,0402,TR
C66000	6010B0136301	CAPACITOR-AL-SP,330UF,2V,-35%/+10%,105C,DX1.9,SMD,TR,9MOHM	C66000	6010B0219101	SP,220UF,2V,M,105C,DX1.9,SMD,TR,6MOHM

# INVENTEC

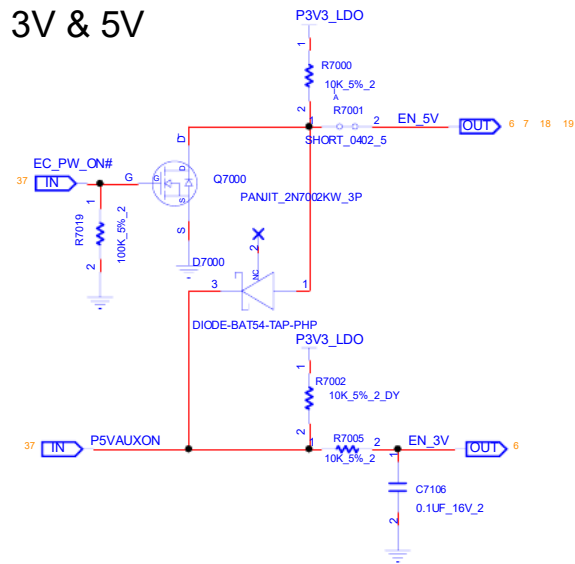
TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE	CODE	DOCNUMBER	REV
A3	CS	1310A29944-0-0	X01
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CHANGE by	Loren Huang	DATE	13-Dec-2017
PCB PN	6050A2994401	PCB VER	X01

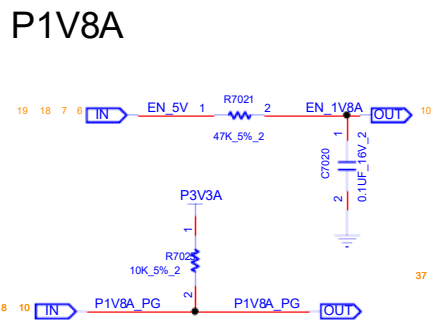


CHANGE by	Loren Huang	DATE	13-Dec.-2017
PCB P/N	6050A2994401	PCB VER	X01

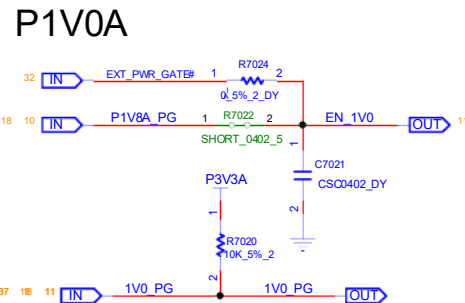
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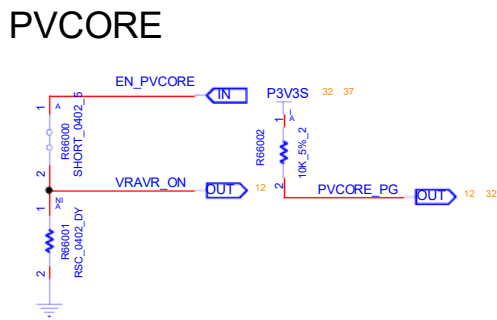
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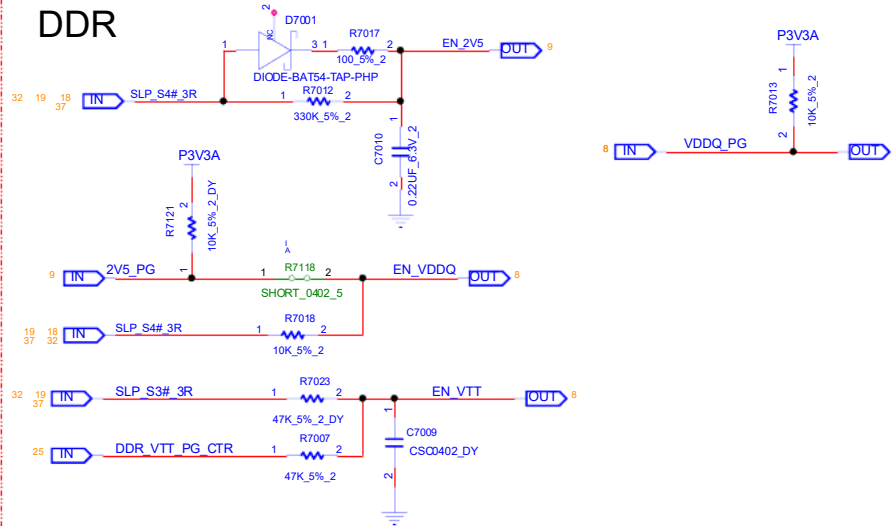
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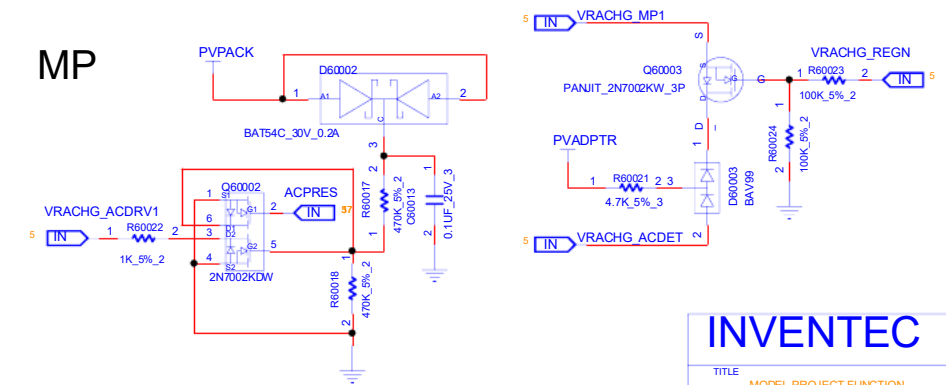
## PVCORE



## DDR



## MP



INVENTEC

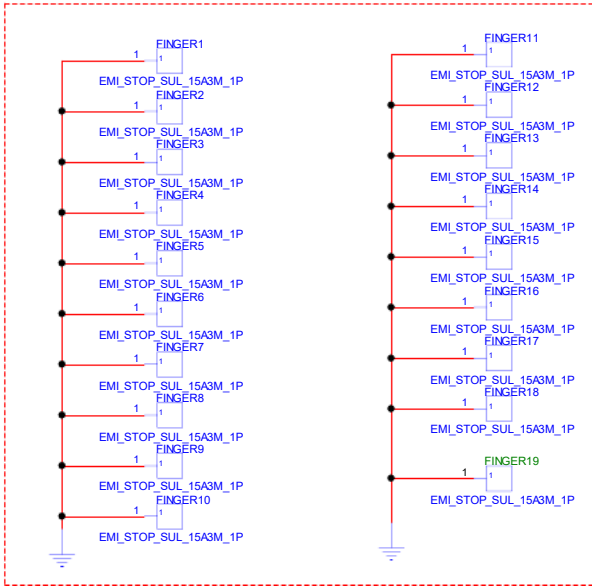
TITLE			
MODEL PROJECT FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310A29944-0-0	X01
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CHANGE by	Loren Huang	DATE	13-Dec.-2017
PCB PIN	6050A2994401	PCB VER	X01

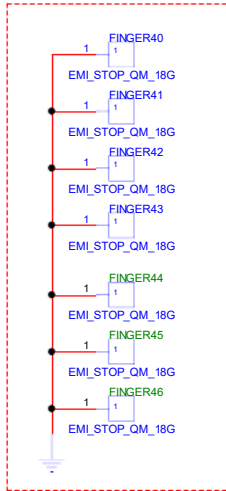


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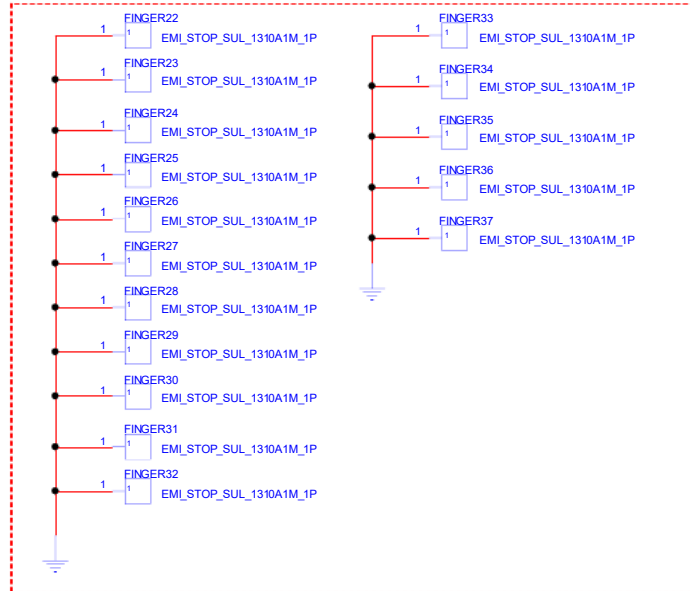
FOR DRAM/VRAM USE



FOR GPU USE



FOR IO USE



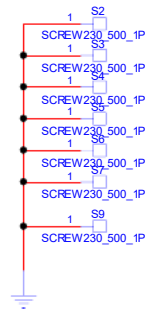
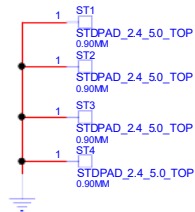
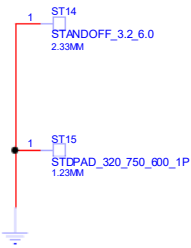
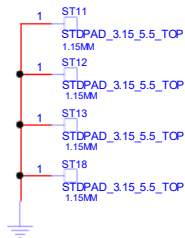
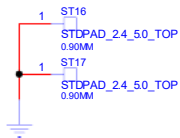
GPU

FAN

SSD

CPU

PCB

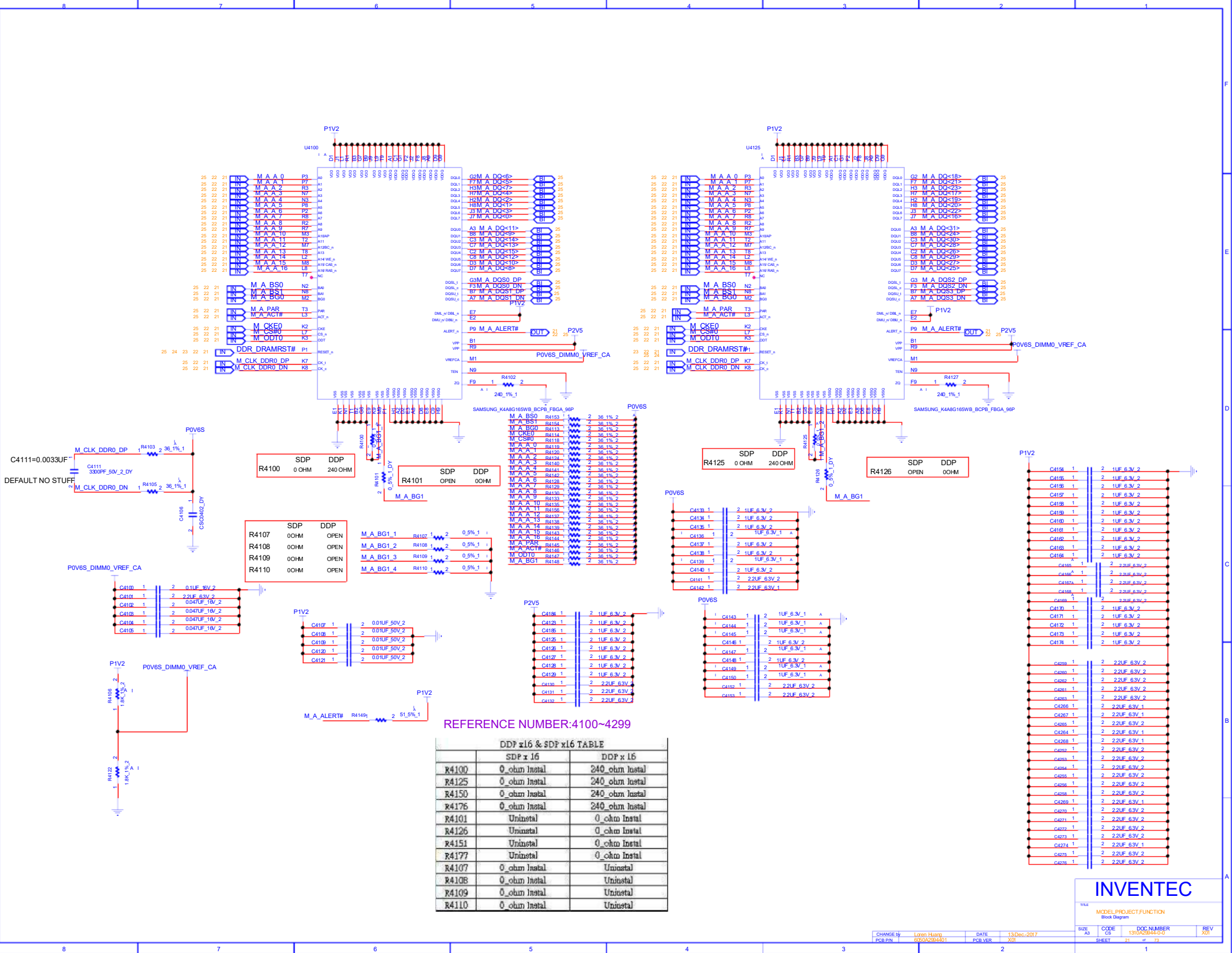


INVENTEC

TITLE  
MODEL PROJECT FUNCTION  
Block Diagram

SIZE A3 CODE CS DOC NUMBER 1310A29944-0-0 REV X01  
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CHANGE by Loren Huang DATE 13-Dec-2017  
PCB PIN 6050A2994401 PCB VER X01



REFERENCE NUMBER:4100~4299

DDP x16 & SDP x16 TABLE		
	SDP x 16	DDP x 16
R4100	0_ohm Instal	240_ohm Instal
R4125	0_ohm Instal	240_ohm Instal
R4150	0_ohm Instal	240_ohm Instal
R4176	0_ohm Instal	240_ohm Instal
R4101	Uninstal	0_ohm Instal
R4126	Uninstal	0_ohm Instal
R4151	Uninstal	0_ohm Instal
R4177	Uninstal	0_ohm Instal
R4107	0_ohm Instal	Uninstal
R4108	0_ohm Instal	Uninstal
R4109	0_ohm Instal	Uninstal
R4110	0_ohm Instal	Uninstal

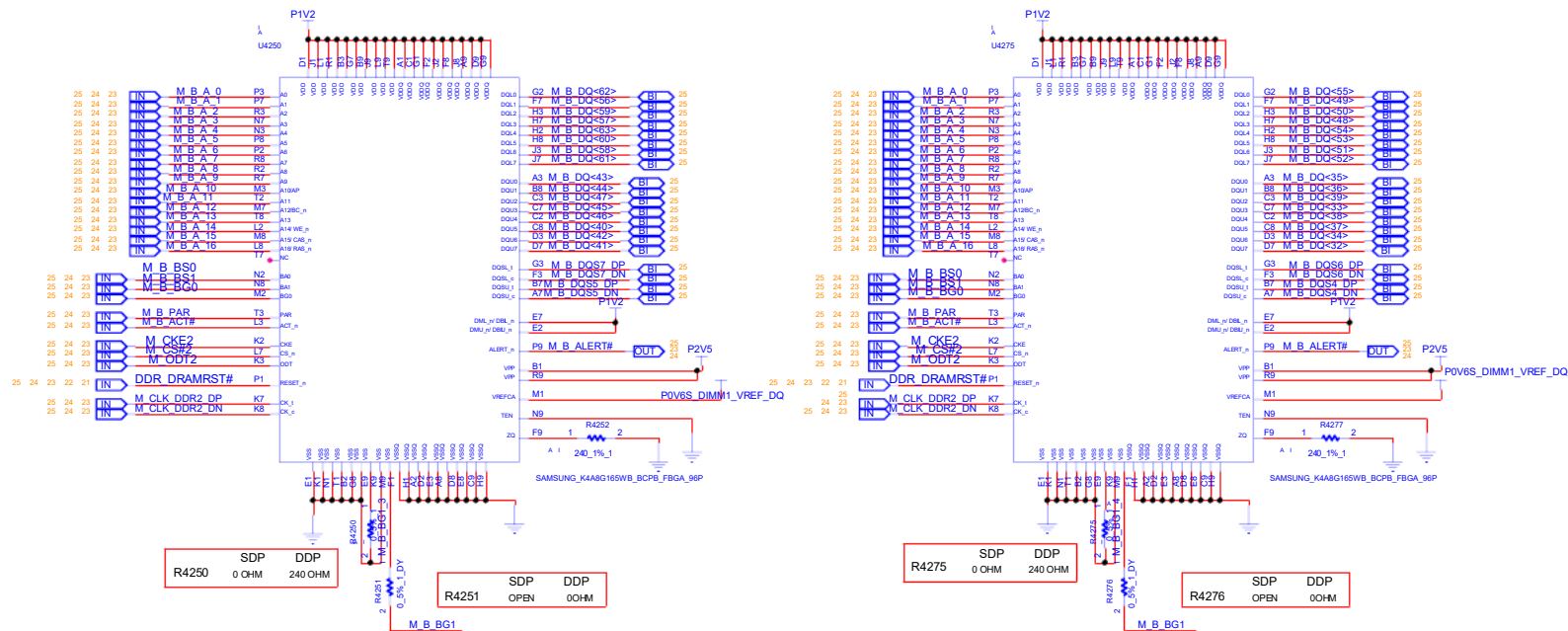
INVENTEC



F



INVENTEC



REFERENCE NUMBER:4100~4299

DDPx16 & SDPx16 TABLE		
	SDPx 16	DDPx 16
R4200	0_ohm Instal	240_ohm Instal
R4225	0_ohm Instal	240_ohm Instal
R4250	0_ohm Instal	240_ohm Instal
R4275	0_ohm Instal	240_ohm Instal
R4201	Uninstal	0_ohm Instal
R4226	Uninstal	0_ohm Instal
R4251	Uninstal	0_ohm Instal
R4276	Uninstal	0_ohm Instal
R4205	0_ohm Instal	Uninstal
R4206	0_ohm Instal	Uninstal
R4207	0_ohm Instal	Uninstal
R4208	0_ohm Instal	Uninstal



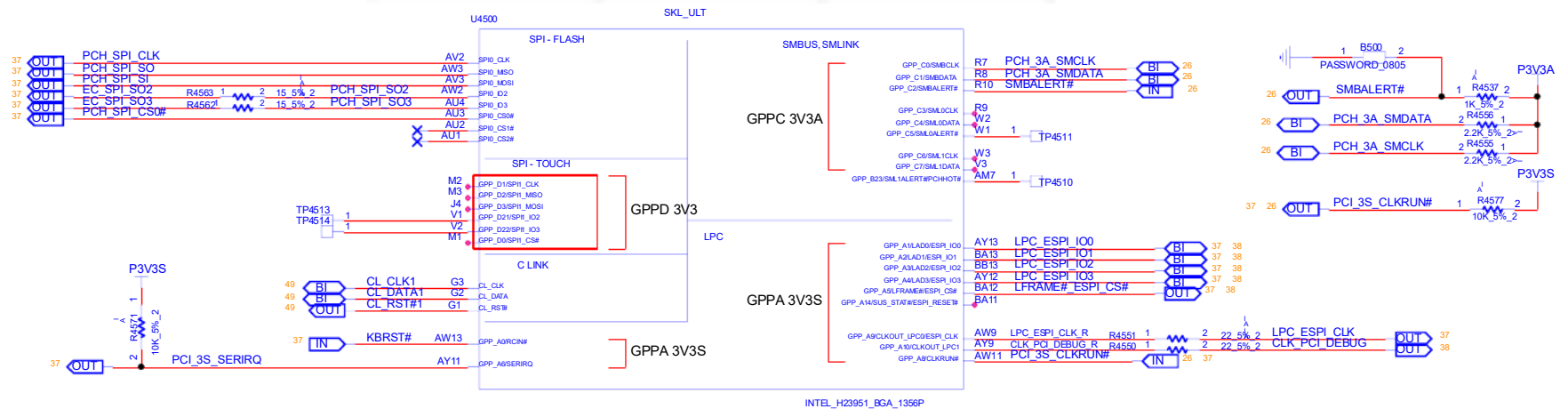


543016 60.3.31: ALL UNUSED GPIOs (WHICH DEFAULT TO GPIO FUNCTIONALITY) DO NOT NEED TERMINATION

All GPIOs have weak internal pull-up/pull-down resistors which are off by default. The internal PU/PD can be programmed (PU/PD/None) by BIOS after reset.

#### GPIO Group Summary

GPIO Group	Power Pins	Voltage
Primary Well Group A (GPP_A)	VCCPGPPA	1.8V or 3.3V
Primary Well Group B (GPP_B)	VCCPGPPB	1.8V or 3.3V
Primary Well Group C (GPP_C)	VCCPGPPC	1.8V or 3.3V
Primary Well Group D (GPP_D)	VCCPGPPD	1.8V or 3.3V
Primary Well Group E (GPP_E)	VCCPGPPE	1.8V or 3.3V
Primary Well Group F (GPP_F)	VCCPGPPF	1.8V
Primary Well Group G (GPP_G)	VCCPGPPG	1.8V or 3.3V
Deep Sleep Well Group (GPD)	VCCPD9W_3p3	3.3V



INVENTEC

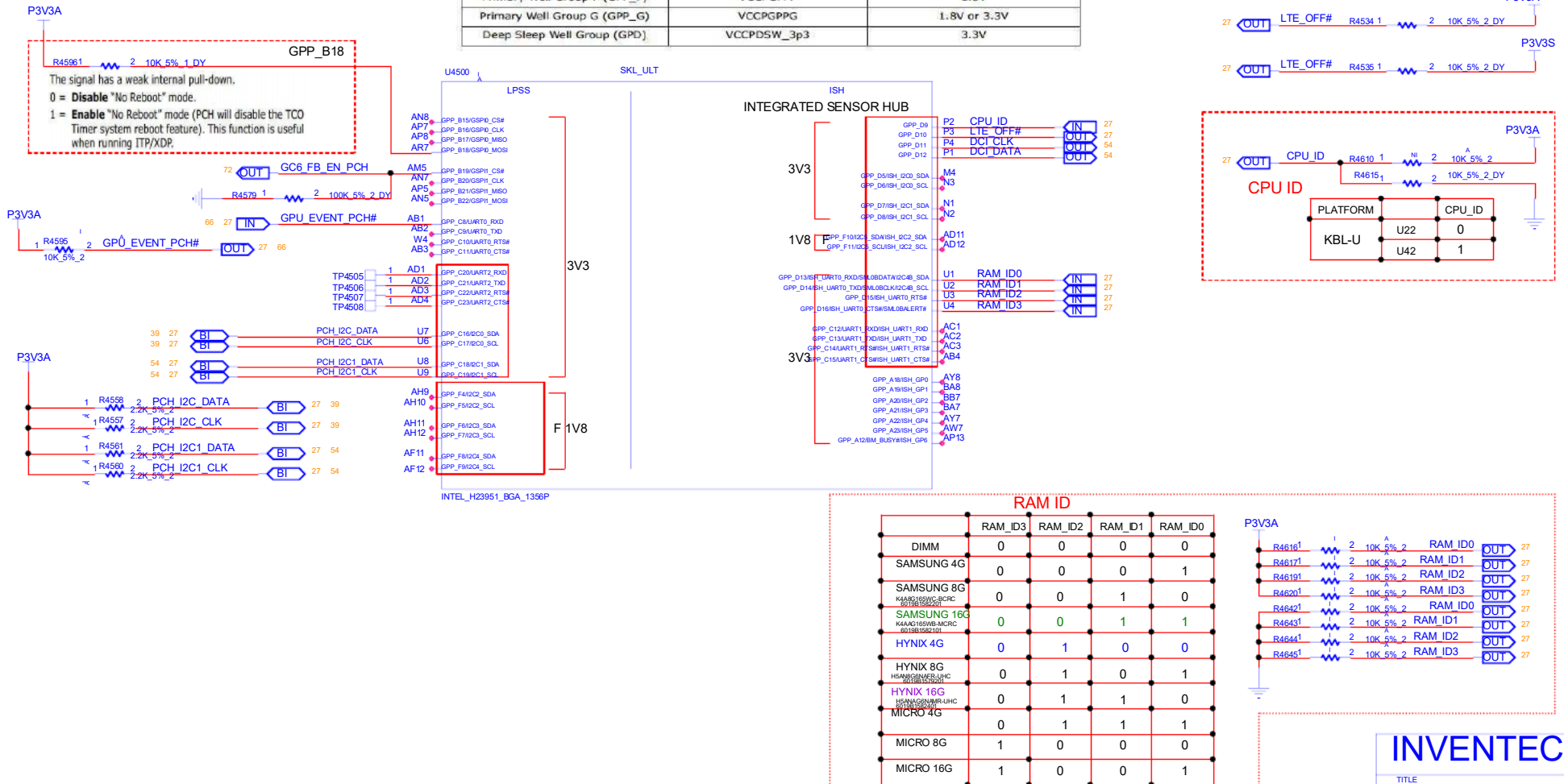
TITLE	MODEL PROJECT FUNCTION	Block Diagram
SIZE	CODE	DOC NUMBER
A3	CS	1310A29944-0-0
SHEET	26	of 73
REV	X01	

CHANGE by	6RNGHuang	DATE	13-Dec.-2017
PCB PN	6050A2994401	PCB VER	X01R>

All GPIOs have weak internal pull-up/pull-down resistors which are off by default. The internal PU/PD can be programmed (PU/PD/None) by BIOS after reset.

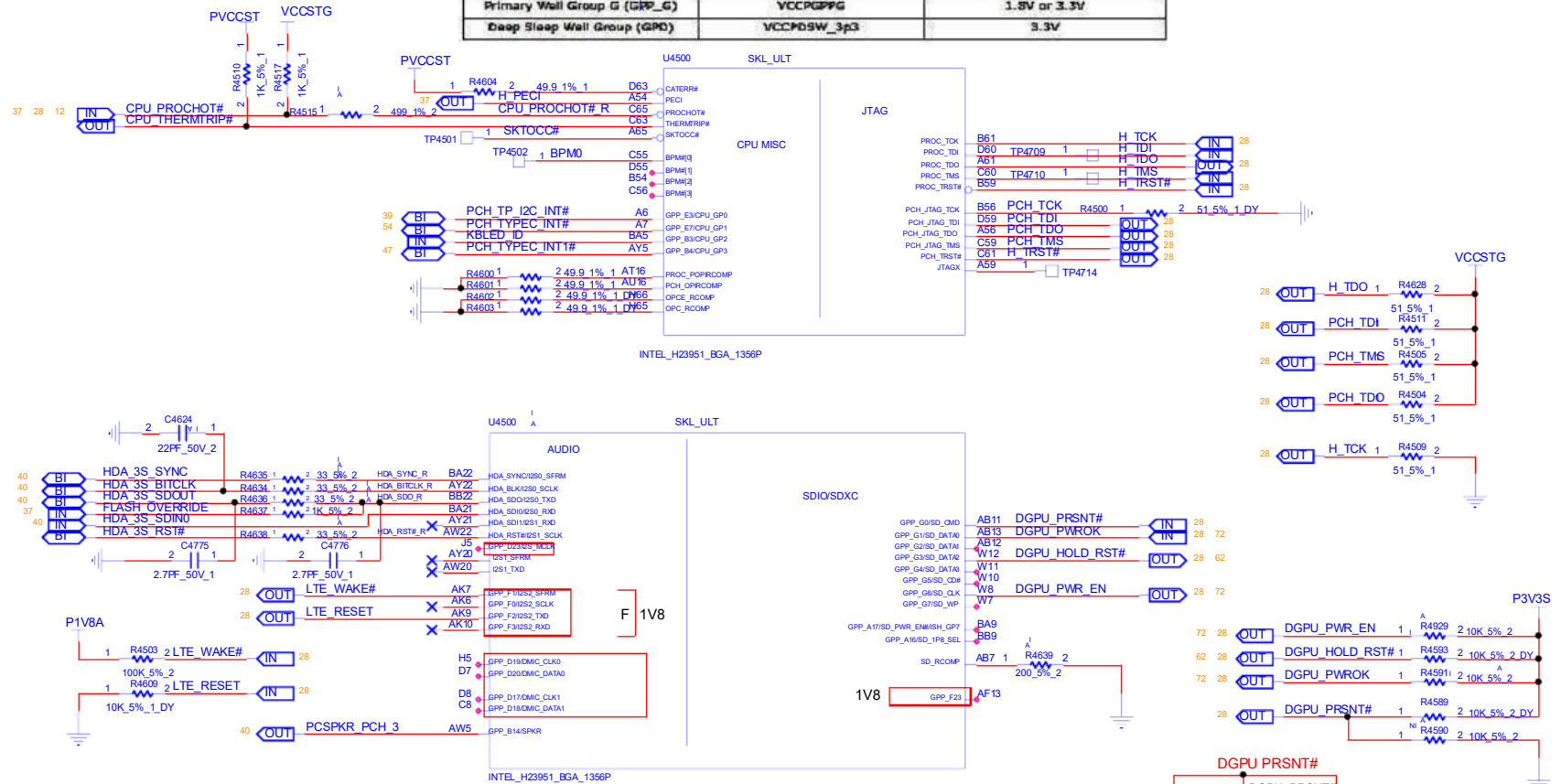
**GPIO Group Summary**

GPIO Group	Power Pins	Voltage
Primary Well Group A (GPP_A)	VCCPGPPA	1.8V or 3.3V
Primary Well Group B (GPP_B)	VCCPGPPB	1.8V or 3.3V
Primary Well Group C (GPP_C)	VCCPGPPC	1.8V or 3.3V
Primary Well Group D (GPP_D)	VCCPGPPD	1.8V or 3.3V
Primary Well Group E (GPP_E)	VCCPGPPE	1.8V or 3.3V
Primary Well Group F (GPP_F)	VCCPGPPF	1.8V
Primary Well Group G (GPP_G)	VCCPGPPG	1.8V or 3.3V
Deep Sleep Well Group (GPD)	VCCPD5W_3p3	3.3V



All GPIOs have weak internal pull-up/pull-down resistors which are off by default. The internal PU/PD can be programmed (PU/PD/None) by BIOS after reset.

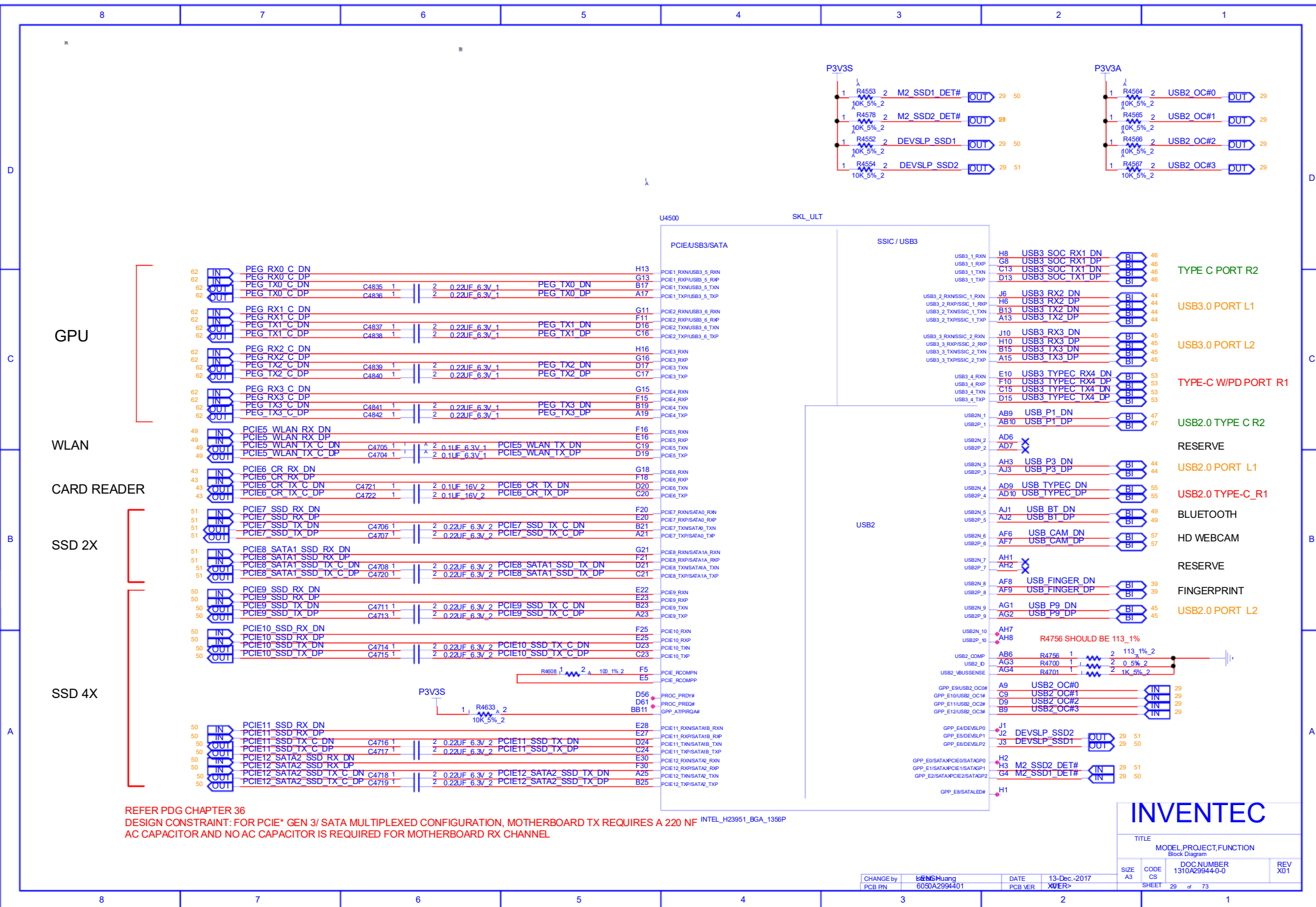
GPIO Group	Power Pins	Voltage
Primary Well Group A (GPP_A)	VCCPGPPA	1.8V or 3.3V
Primary Well Group B (GPP_B)	VCCPGPPB	1.8V or 3.3V
Primary Well Group C (GPP_C)	VCCPGPPC	1.8V or 3.3V
Primary Well Group D (GPP_D)	VCCPGPPD	1.8V or 3.3V
Primary Well Group E (GPP_E)	VCCPGPPE	1.8V or 3.3V
Primary Well Group F (GPP_F)	VCCPGPPF	1.8V
Primary Well Group G (GPP_G)	VCCPGPPG	1.8V or 3.3V
Deep Sleep Well Group (GPD)	VCCPD5W_3p3	3.3V



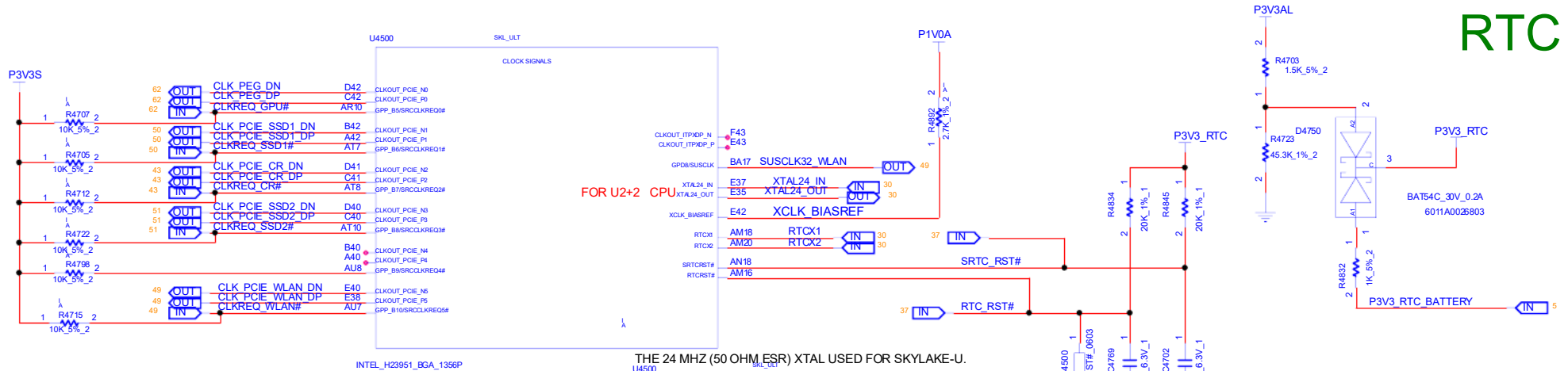
DGPU PRSNT#	
	DGPU_PRSN
DIS	0
UMA	1

TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310A29944-0-0	REV X01
SHEET 28 of 73			

CHANGE by	LENG Huang	DATE	13-Dec-2017
PCB P/N	6050A2994401	PCB VER	XVER>



RTC

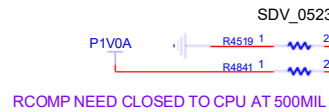


FOR U2+2 CPU

THE 24 MHZ (50 OHM ESR) XTAL USED FOR SKYLAKE-U.

STRAPPING:  
DP ENABLE/DISABLE  
0 : ENABLED

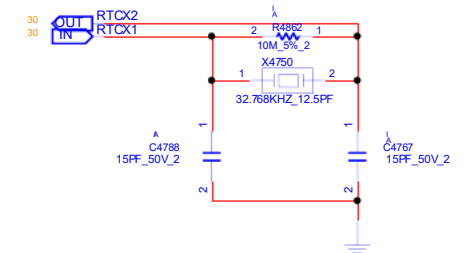
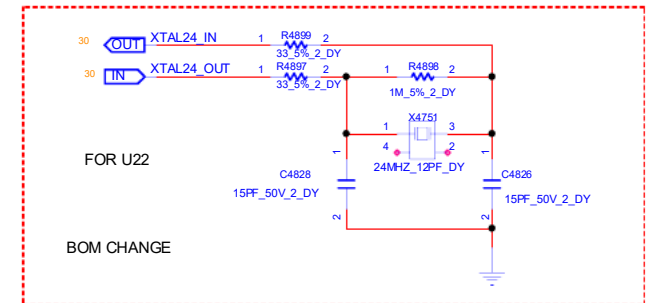
Processor strap CFG[4] should be pulled low to enable embedded DisplayPort\*



RCOMP NEED CLOSED TO CPU AT 500MIL

SRCCLKRQ[5:0]# CAN BE ASSIGNED TO DIFFERENT SRC CLOCKS USING FW SETTINGS AND MAY NOT NECESSARILY CORRESPOND TO THE SAME PCI EXPRESS CLOCK NUMBER  
ROOT PORTS WHILE USING ANY OF THE CLKOUT\_SRC\_P# DIFFERENTIAL PAIRS.

REFERENCE:4500~4949



INVENTEC

TITLE			
MODEL PROJECT:FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310A29944-0-0	X01
SHEET		of 30	73

CHANGE by  
PCB DN

Loren Huang  
665032994401

DATE  
PCB VER

DATE  
PCB VER

DATE  
PCB VER

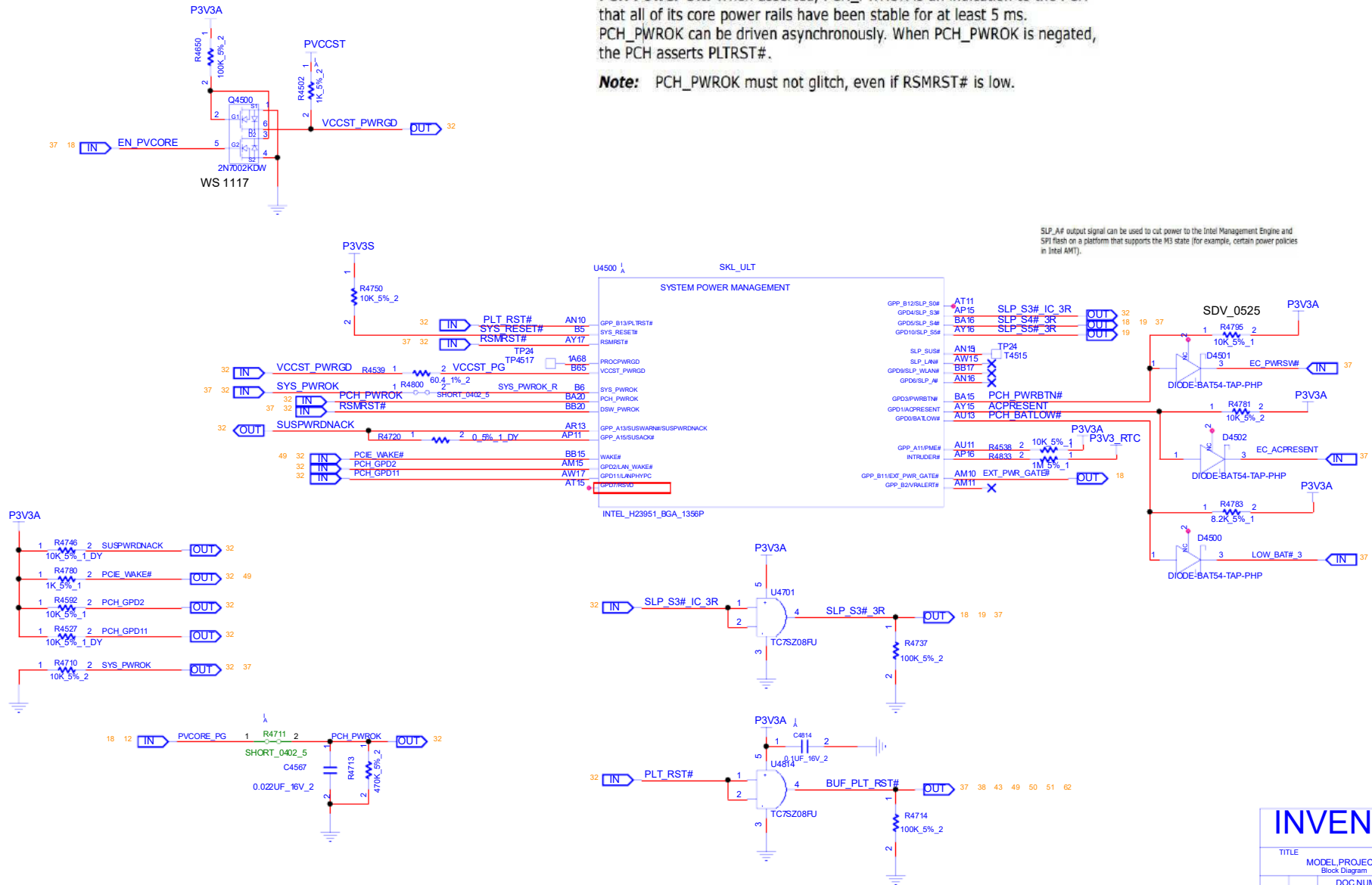




**PCH Power OK:** When asserted, PCH\_PWROK is an indication to the PCH that all of its core power rails have been stable for at least 5 ms. PCH\_PWROK can be driven asynchronously. When PCH\_PWROK is negated, the PCH asserts PLTRST#.

**Note:** PCH\_PWROK must not glitch, even if RSMRST# is low.

SLP\_#F output signal can be used to cut power to the Intel Management Engine and SPI flash on a platform that supports the M3 state (for example, certain power policies in Intel AMT).



INVENTEC

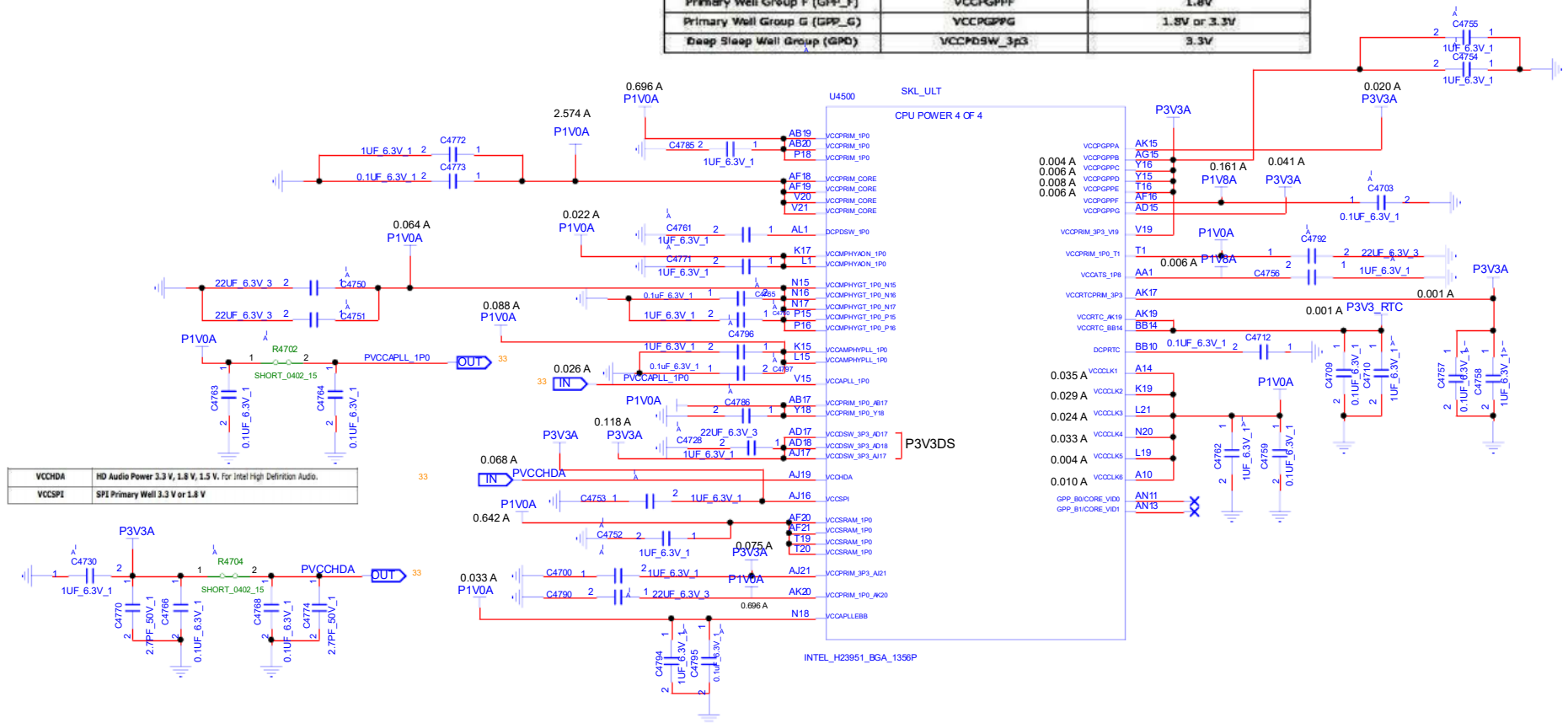
TITLE			
MODEL PROJECT FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310A29944-0-0	X01
SHEET		32 of 73	

CHANGE by	65NGHuang	DATE	13-Dec.-2017
PCB PN	6050A2994401	PCB VER	XVFR>



### GPID Group Summary

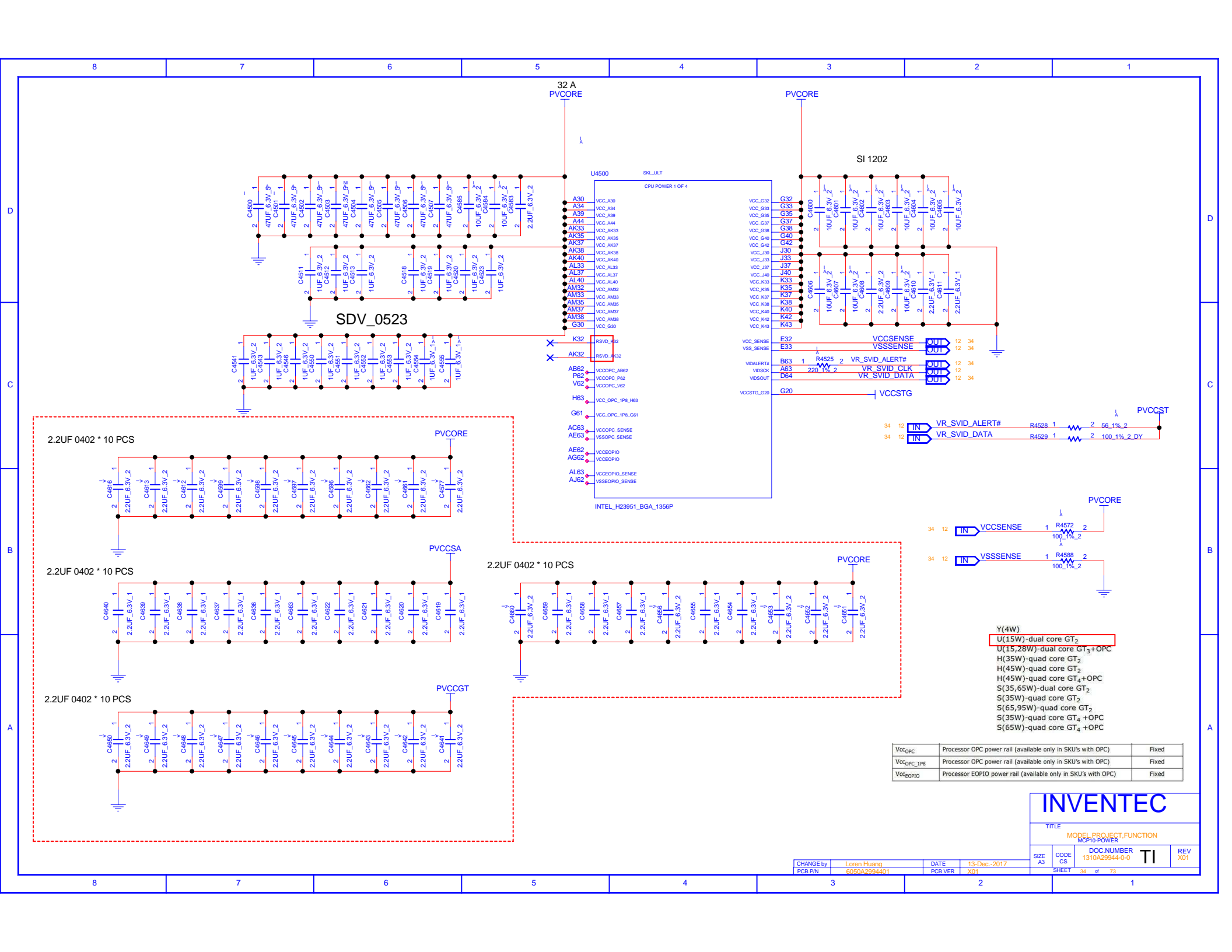
GPIO Group	Power Pins	Voltage
Primary Well Group A (GPP_A)	VCCPGPPA	1.8V or 3.3V
Primary Well Group B (GPP_B)	VCCPGPPB	1.8V or 3.3V
Primary Well Group C (GPP_C)	VCCPGPPC	1.8V or 3.3V
Primary Well Group D (GPP_D)	VCCPGPPD	1.8V or 3.3V
Primary Well Group E (GPP_E)	VCCPGPPE	1.8V or 3.3V
Primary Well Group F (GPP_F)	VCCPGPPF	1.8V
Primary Well Group G (GPP_G)	VCCPGPPG	1.8V or 3.3V
Deep Sleep Well Group (GPD)	VCCPDW_3p3	3.3V



## INVENTEC

TITLE			MODEL,PROJECT,FUNCTION		
			Block Diagram		
SIZE A3	CODE CS	DOC.NUMBER 1310A29944-0-0			
SHEET		of 33		73	

CHANGE by	Loren Huang	DATE	
PCB P/N	66501299-4401	PCB VER	XIV Rev - 2017



VCCOPC	Processor OPC power rail (available only in SKU's with OPC)	Fixed
VCCOPC_IPB	Processor OPC power rail (available only in SKU's with OPC)	Fixed
VCCOPC_EIO	Processor EPIO power rail (available only in SKU's with OPC)	Fixed

INVENTEC

TITLE

MODEL,PROJECT,FUNCTION

MCPI10-POWER

SIZE

A3

CODE

CS

DOC NUMBER

1310A29944-0-0

TI

REV

X01

SHEET

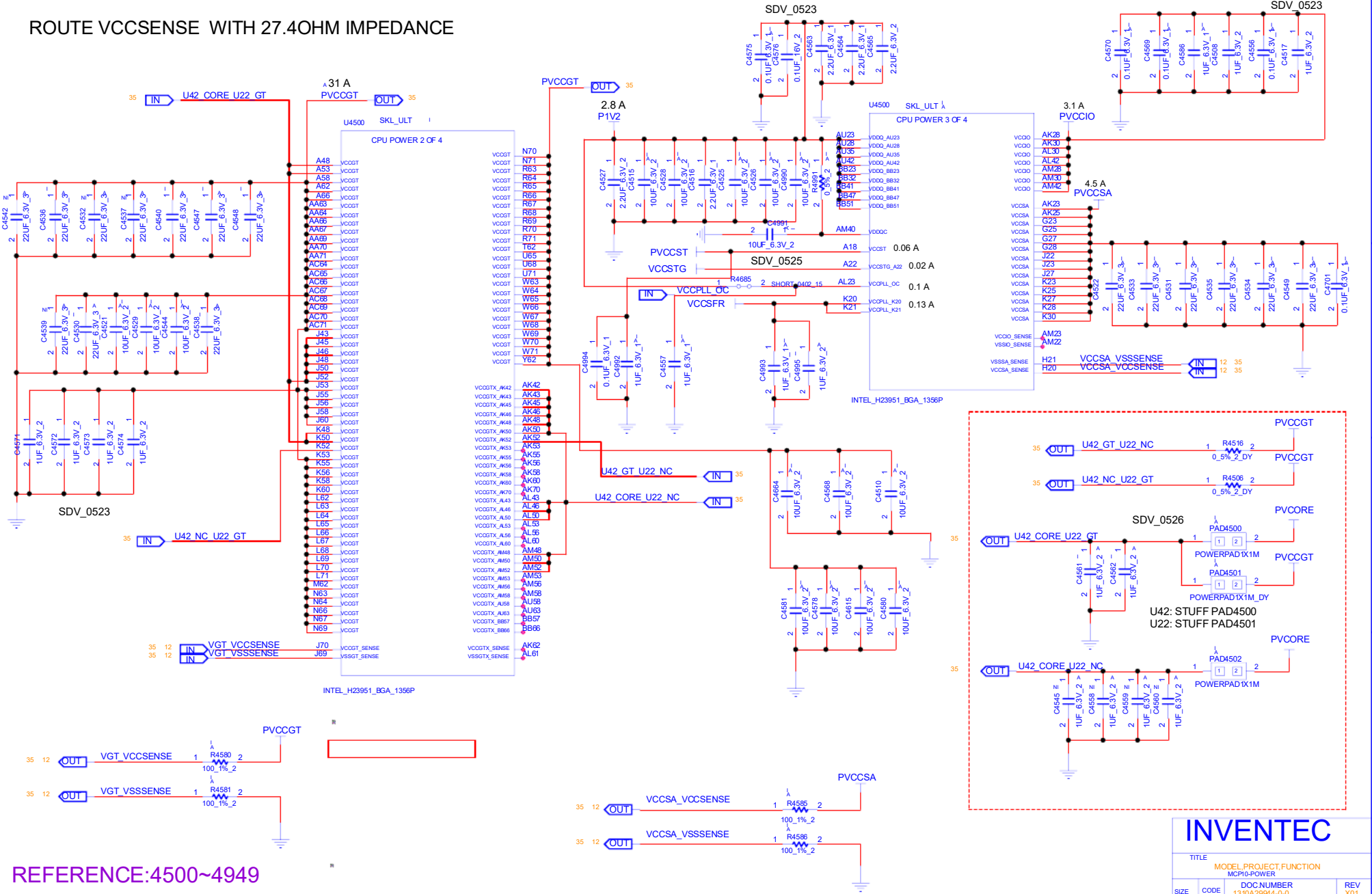
34

of

73

CHANGE by	Loren Huang	DATE	13-Dec-2017
PCB P/N	6050A2994401	PCB VER	X01

# ROUTE VCCSENSE WITH 27.4OHM IMPEDANCE

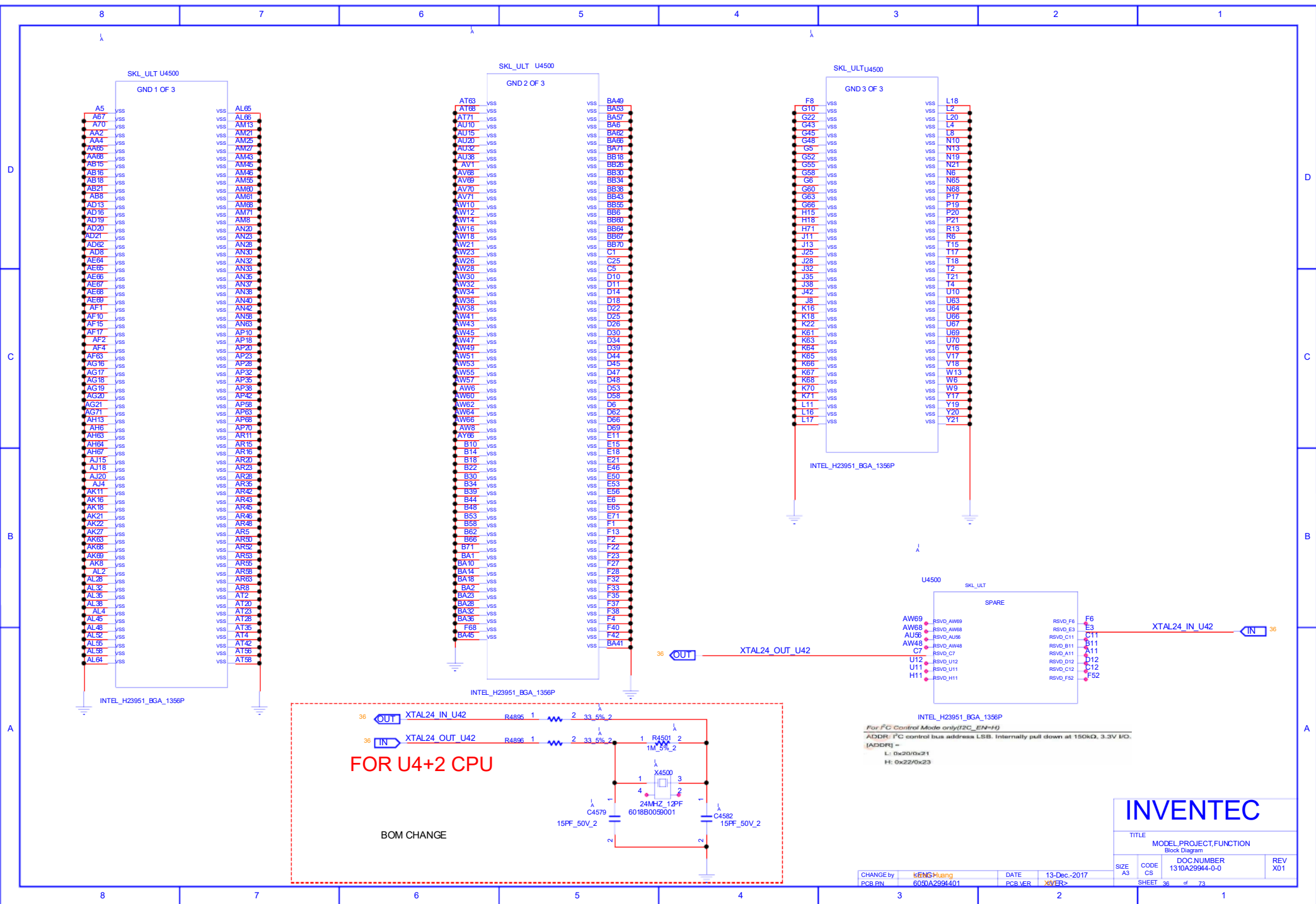


REFERENCE:4500~4949

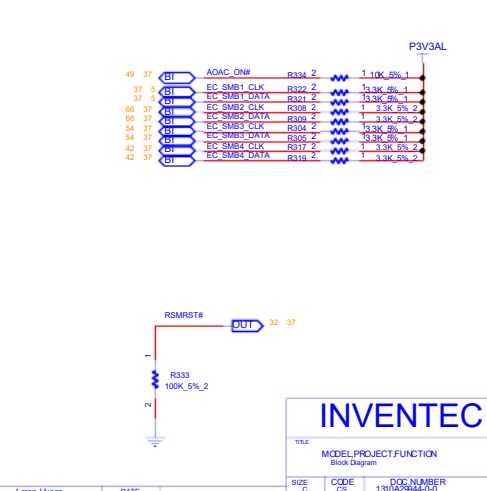
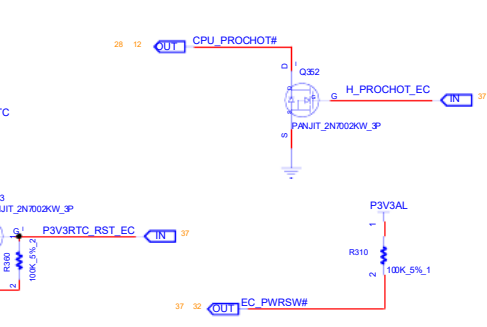
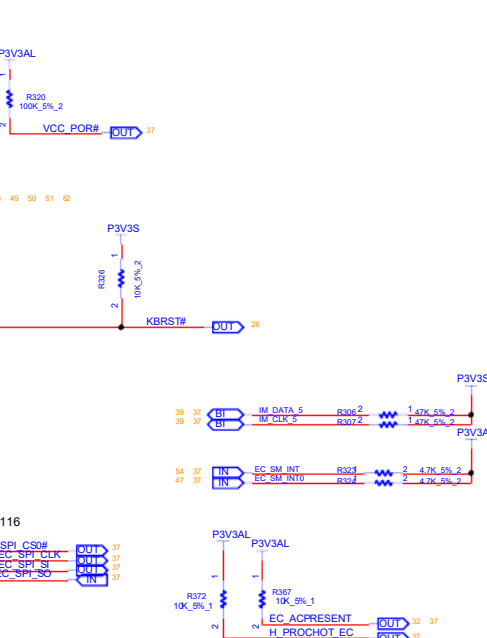
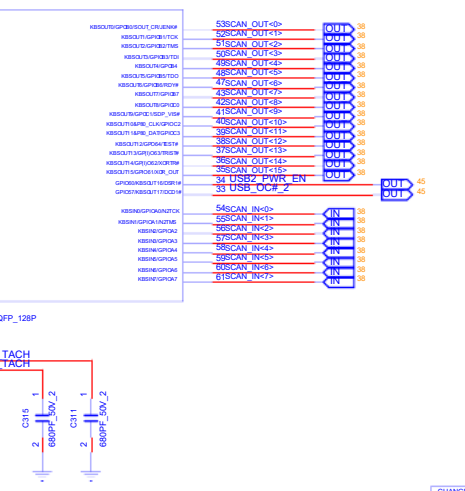
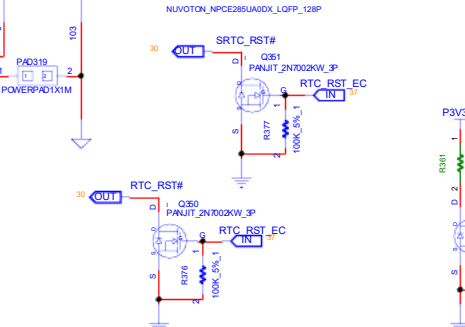
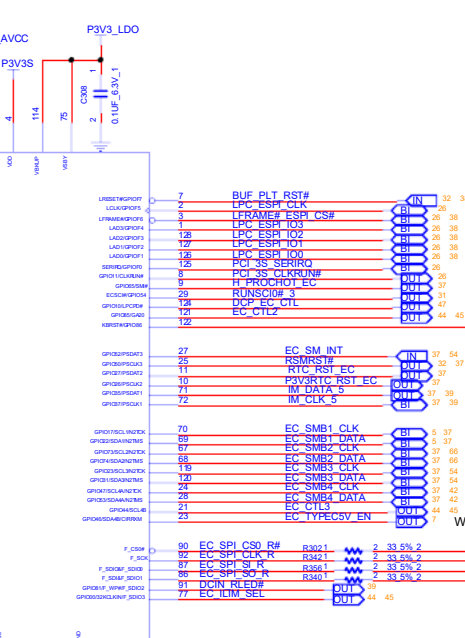
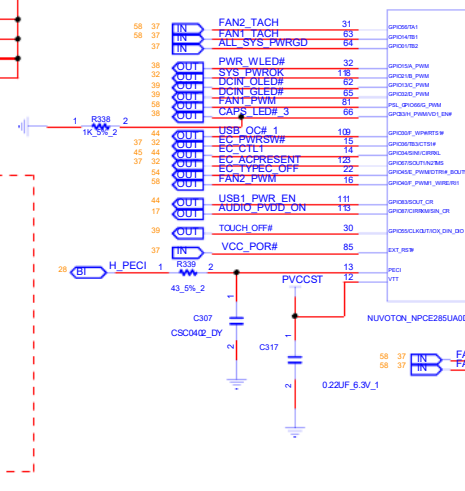
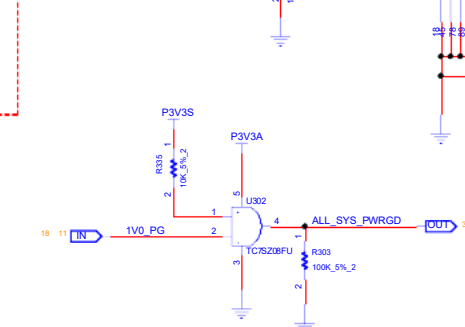
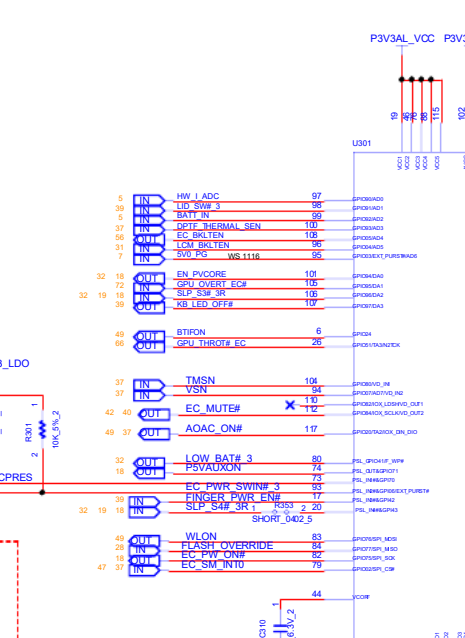
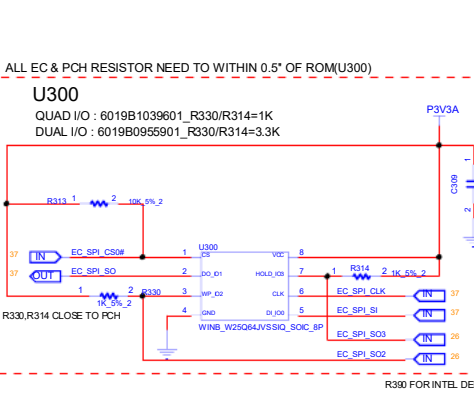
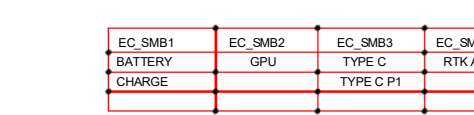
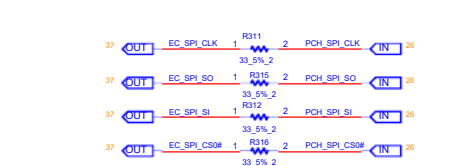
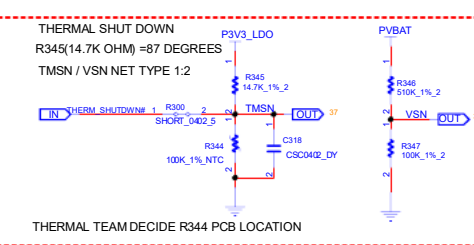
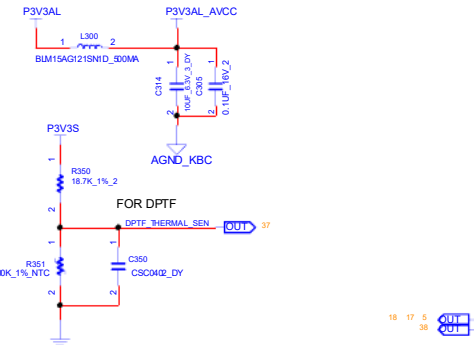
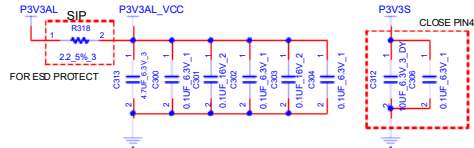
CHANGE by	Loren Huang	DATE	13-Dec-2017
PCB PIN	6050A2994401	PCB VER	X01

INVENTEC

TITLE	MODEL PROJECT FUNCTION	REV	X01
SIZE	CODE	DOC NUMBER	
A3	CS	1310A29944-0-0	
SHEET	35	of	73

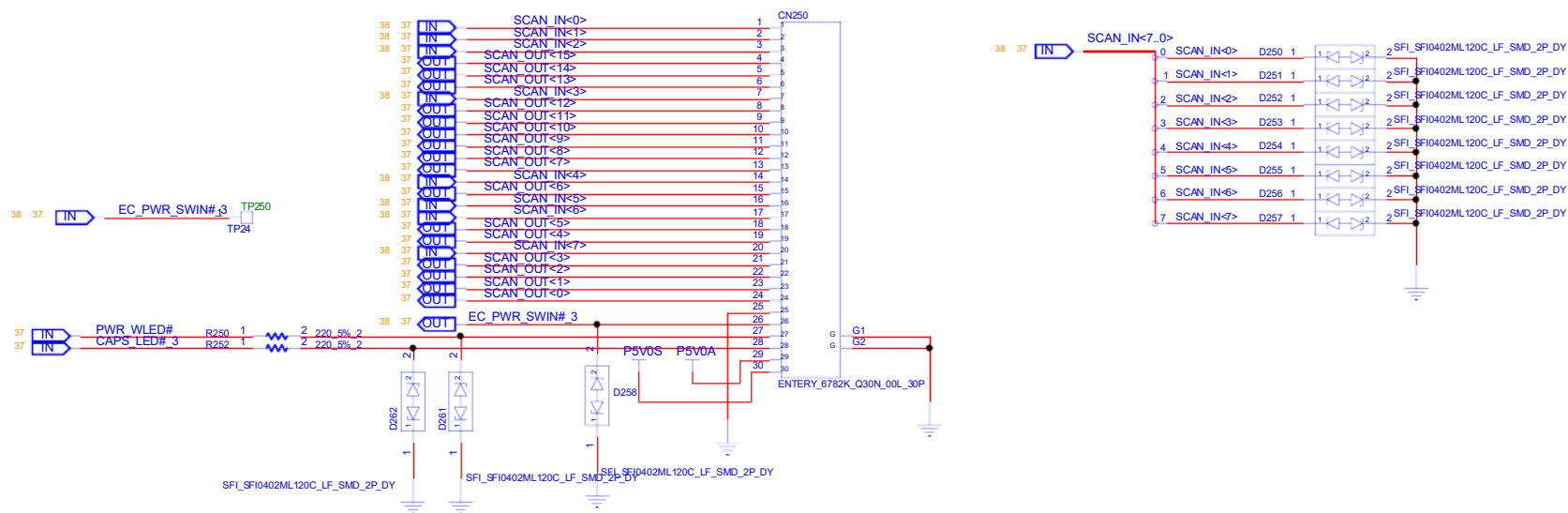


# REFERENCE 300~389(KBC)

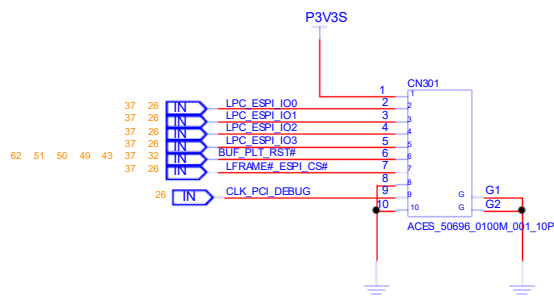


INVENTEC

REFERENCE 200~249(POWER CONN)  
REFERENCE 250~299(KB/TP CONN)



## KEYBOARD CONN

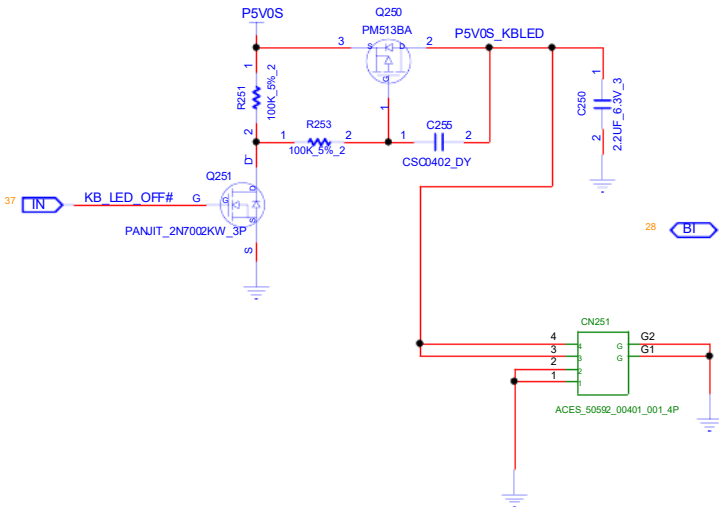
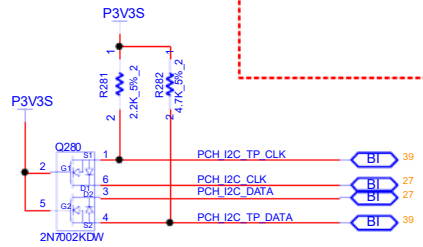
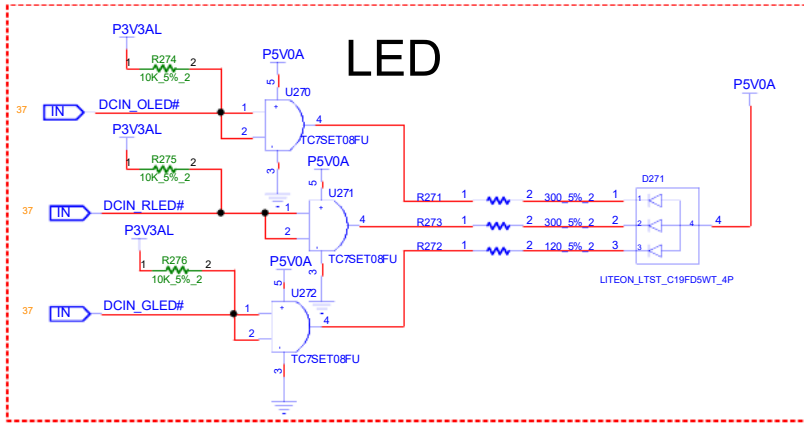
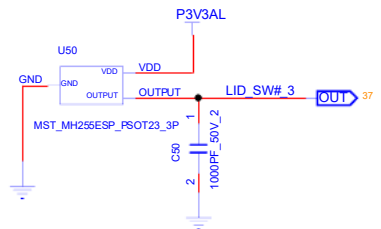


## DEBUG CONN

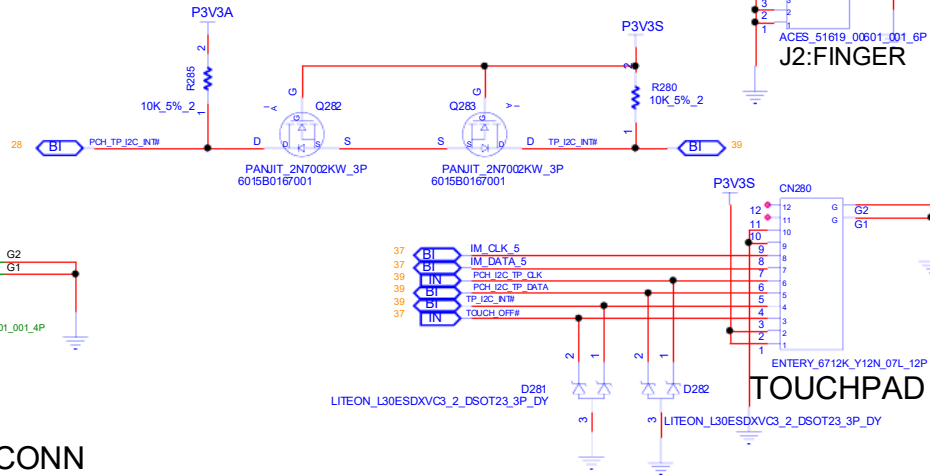
INVENTEC

TITLE			
MODEL PROJECT:FUNCTION Block Diagram			
SIZE A3		DOC NUMBER 1310A29944-0-0	REV X01
SHEET		of 38	73

CHANGE by: **Loren Huang** DATE: **2017.12.14**  
PCB PIN: **66N262994401** PCB VER: **X14**



KEYBOARD LED CONN

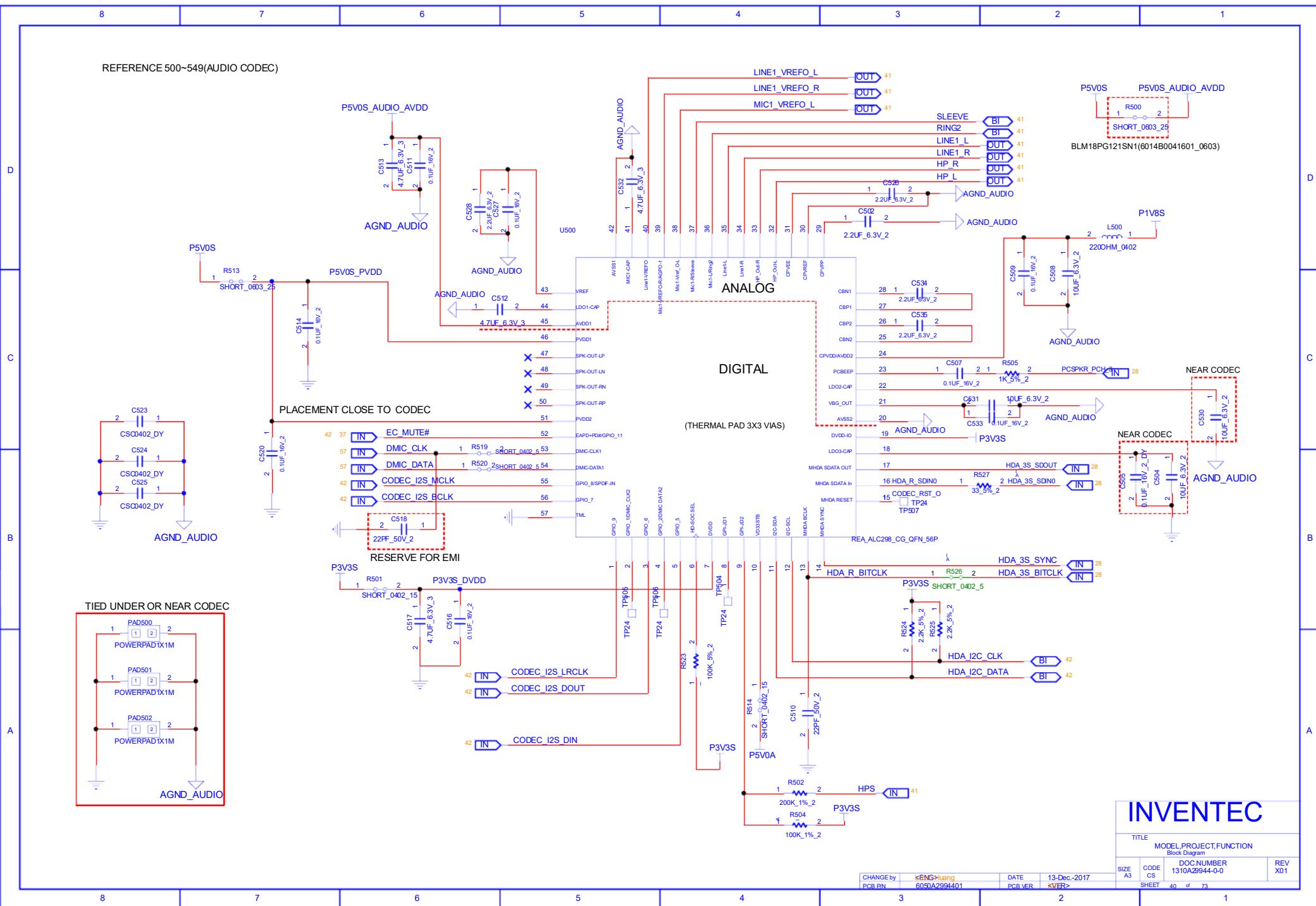


TOUCHPAD CONN (CLICK PAD)

INVENTEC

CHANGE by	Loren Huang	DATE	13-Dec-2017
PCB PIN	6050A2994401	PCB VER	X01

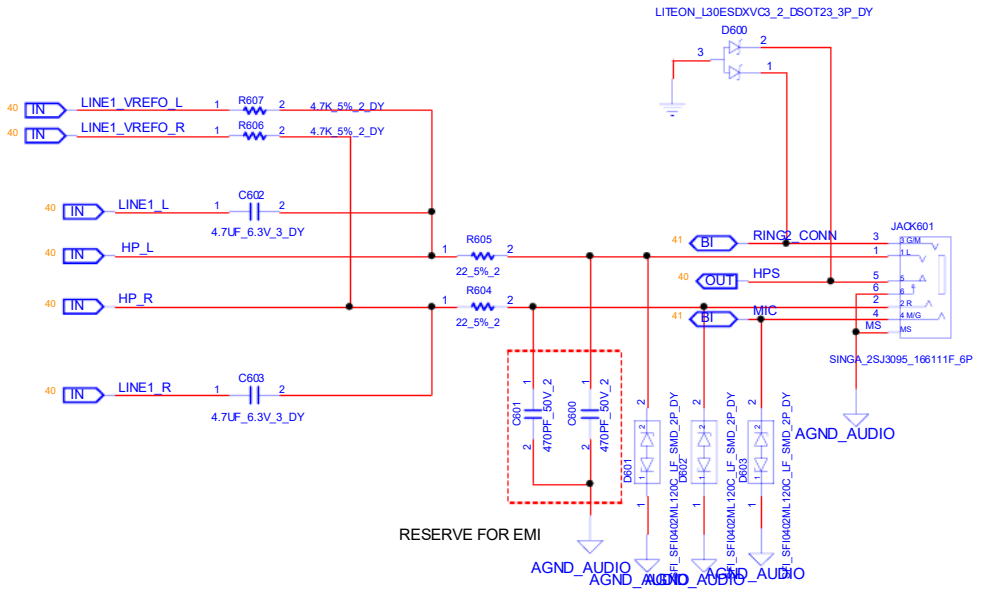
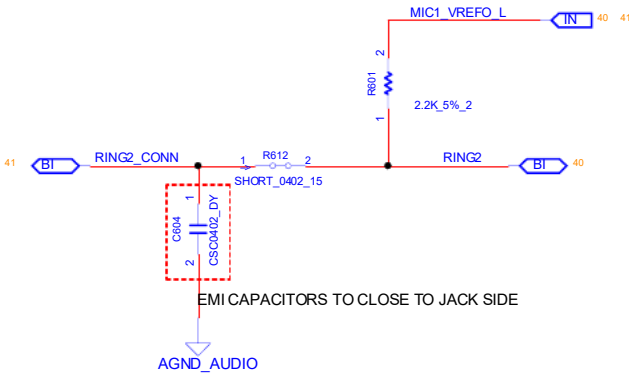
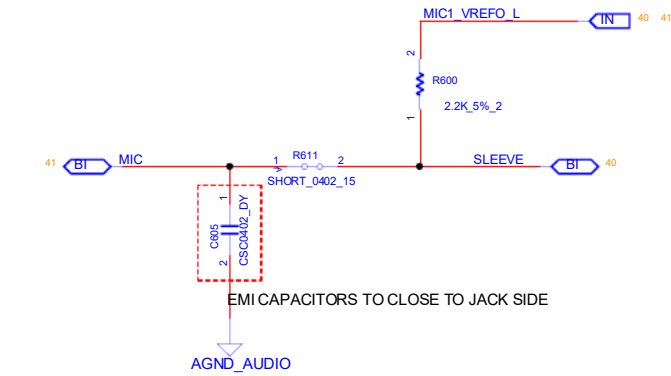
TITLE	MODEL PROJECT,FUNCTION	REV	X01
SIZE	A3	CODE	CS
SHEET	39 of 73	DOCNUMBER	1310A29944-0-0





REFERCE 600~649(JACK/MIC/SPEAKER)

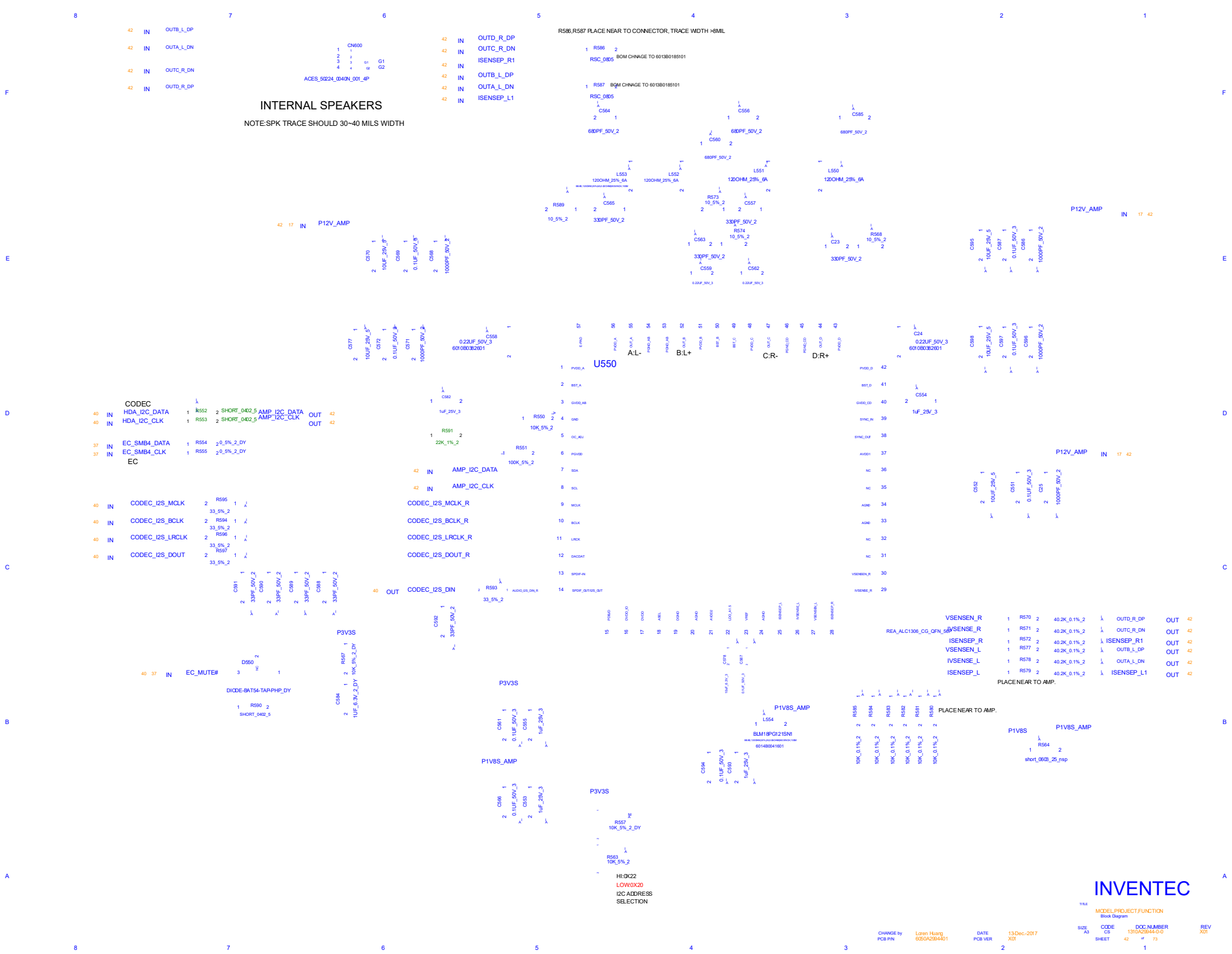
# AUDIO JACKS



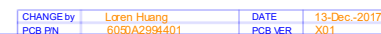
INVENTEC

TITLE			
MODEL PROJECT FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310A29944-0-0	X01
SHEET		41 of 73	

CHANGE by	Loren Huang	DATE	13-Dec-2017
PCB PIN	6050A2994401	PCB VER	X01



## CARD READER

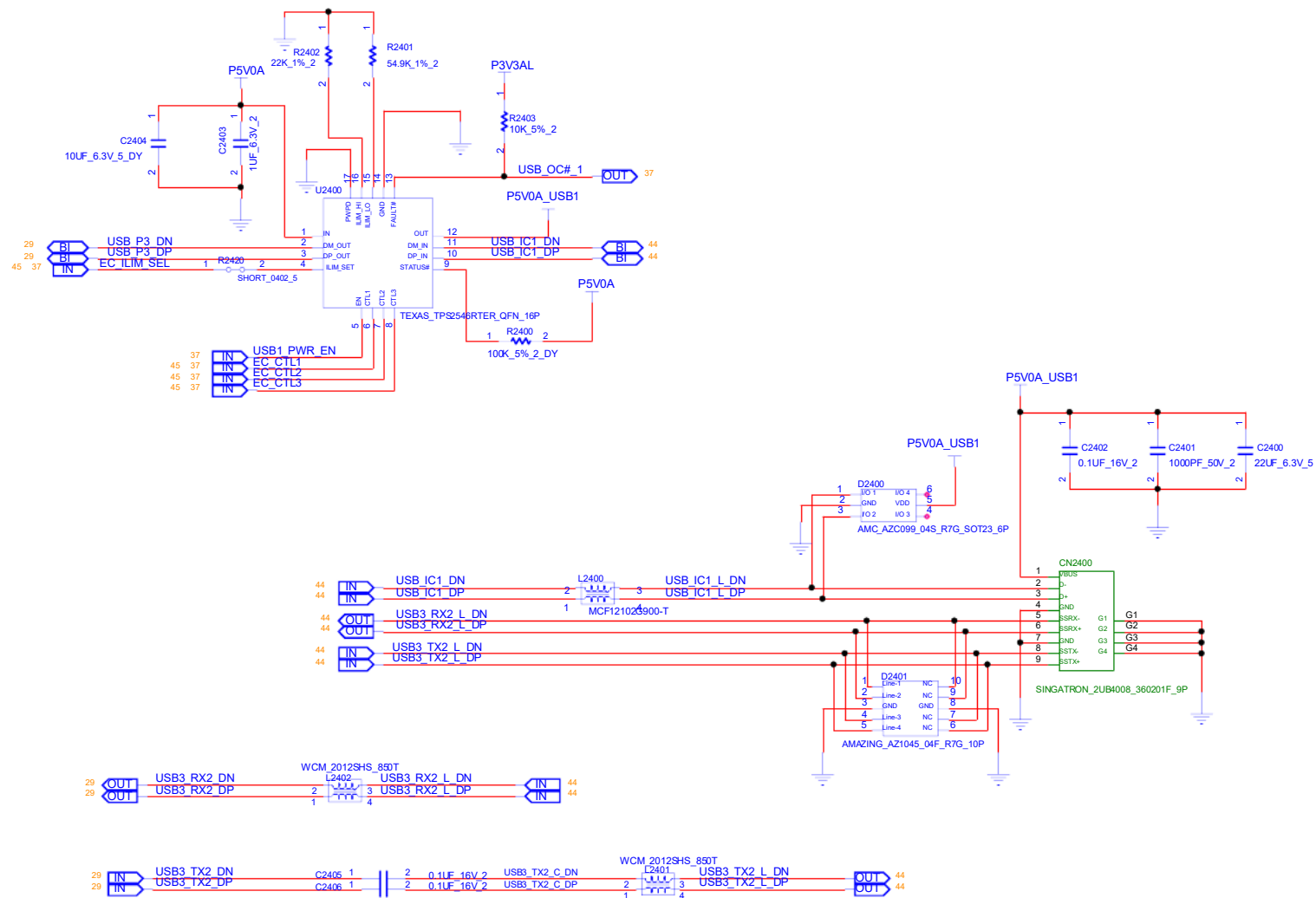


TITLE	MODEL,PROJECT,FUNCTION

SIZE A3	CODE CS	DOC.NUMBER 1310A29944-0-0
SHEET		43 of 73

REFERENCE 2400~2450(USB3.0)

## USB 3.0 PORT1



# INVENTEC

TITLE	MODEL,PROJECT,FUNCTION
	Block Diagram

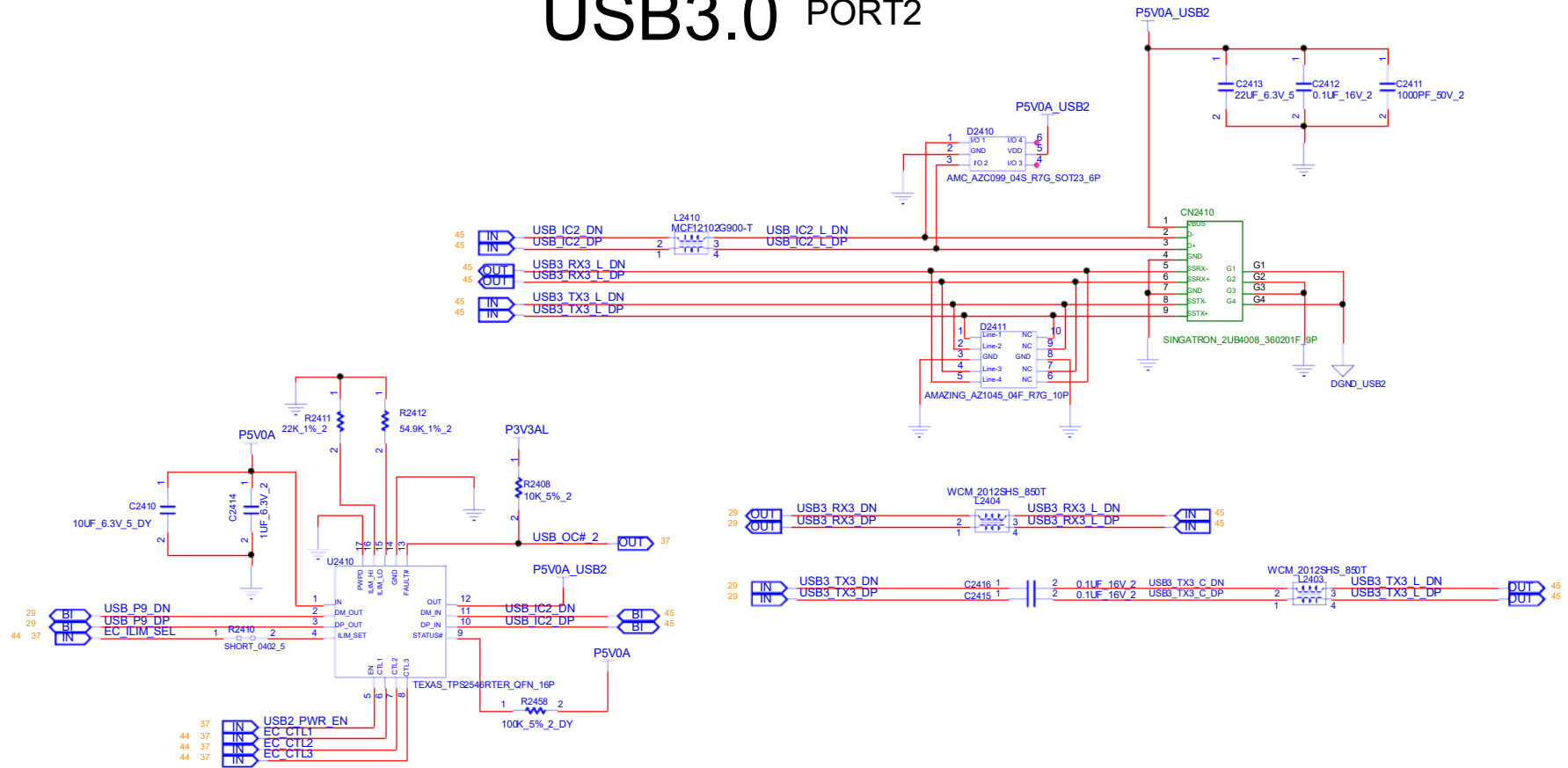
SIZE A3	CODE CS	DOC. NUMBER 1310A29944-0-0
SHEET		44 of 73

REV  
X01

CHANGE by	Loren Huang	DATE	13-Dec.-2017
PCB P/N	6050A2994401	PCB VER	X01

CHANGE by	Loren Huang
PCB P/N	6050A2994401

# USB3.0 PORT2



INVENTEC

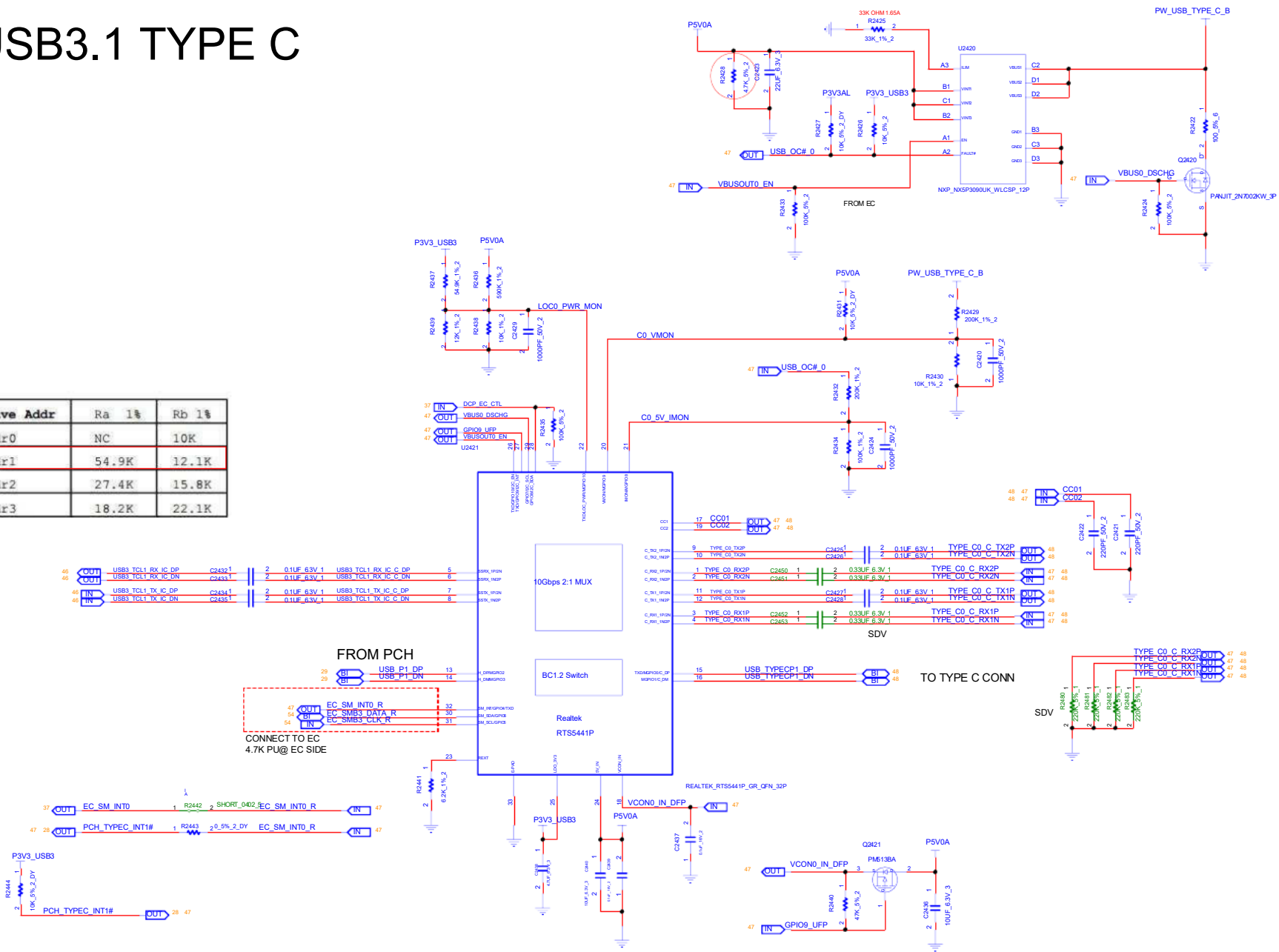
TITLE			
MODEL PROJECT FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310A29944-0-0	X01
SHEET	45	of 73	

CHANGE by	Loren Huang	DATE	13-Dec-2017
PCB DN	6050A2994401	PCB VER	X01



# USB3.1 TYPE C

Slave Addr	Ra 1s	Rb 1s
addr0	NC	10K
addr1	54.9K	12.1K
addr2	27.4K	15.8K
addr3	18.2K	22.1K



CHANGE by	Loren Huang	DATE	13 Dec. 2017
PCB PIN	6050A2994401	PCB VER	KVER>

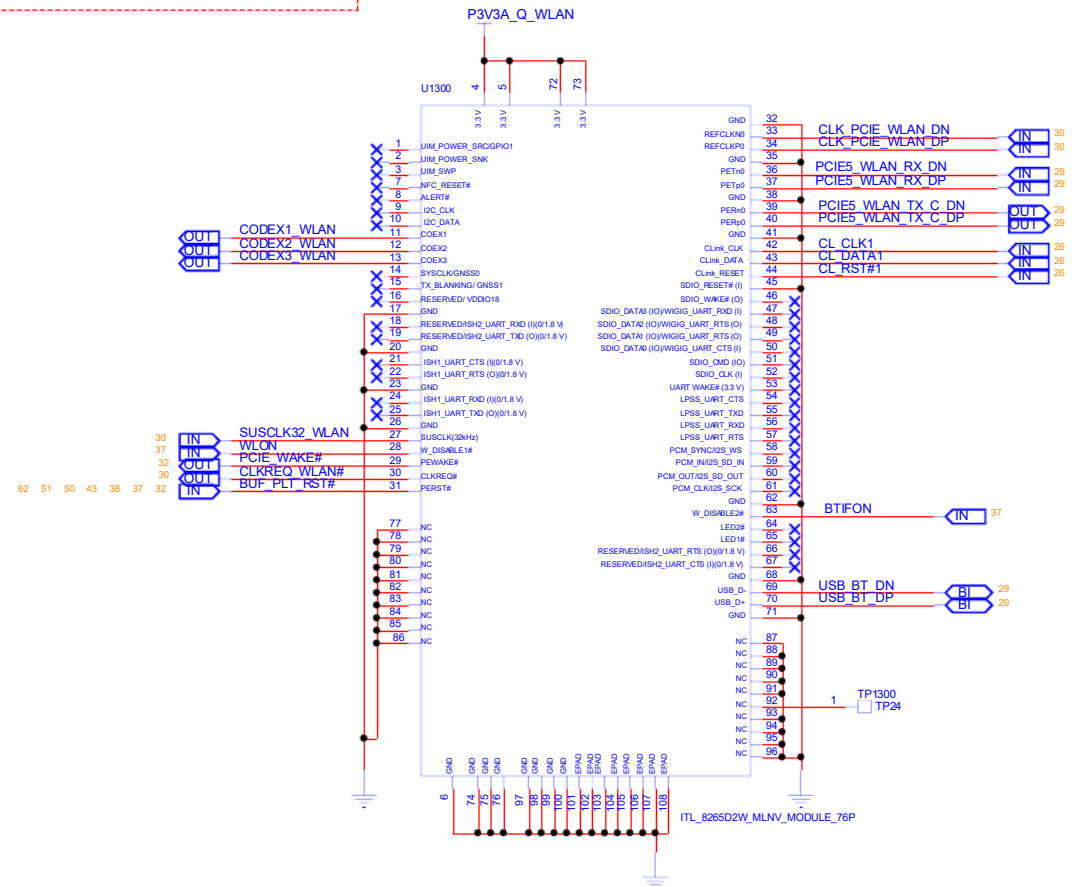
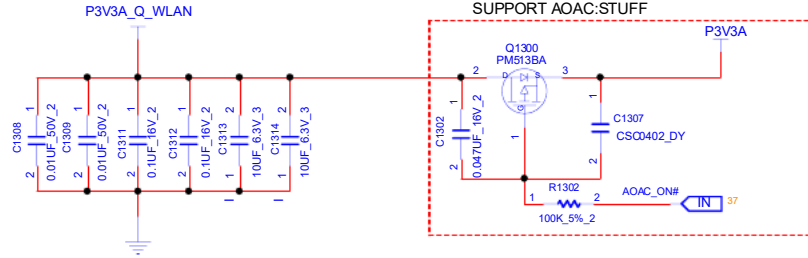


# WLAN

REFERENCE 1300 ~ 1349

(1.1A)

SUPPORT AOAC:STUFF



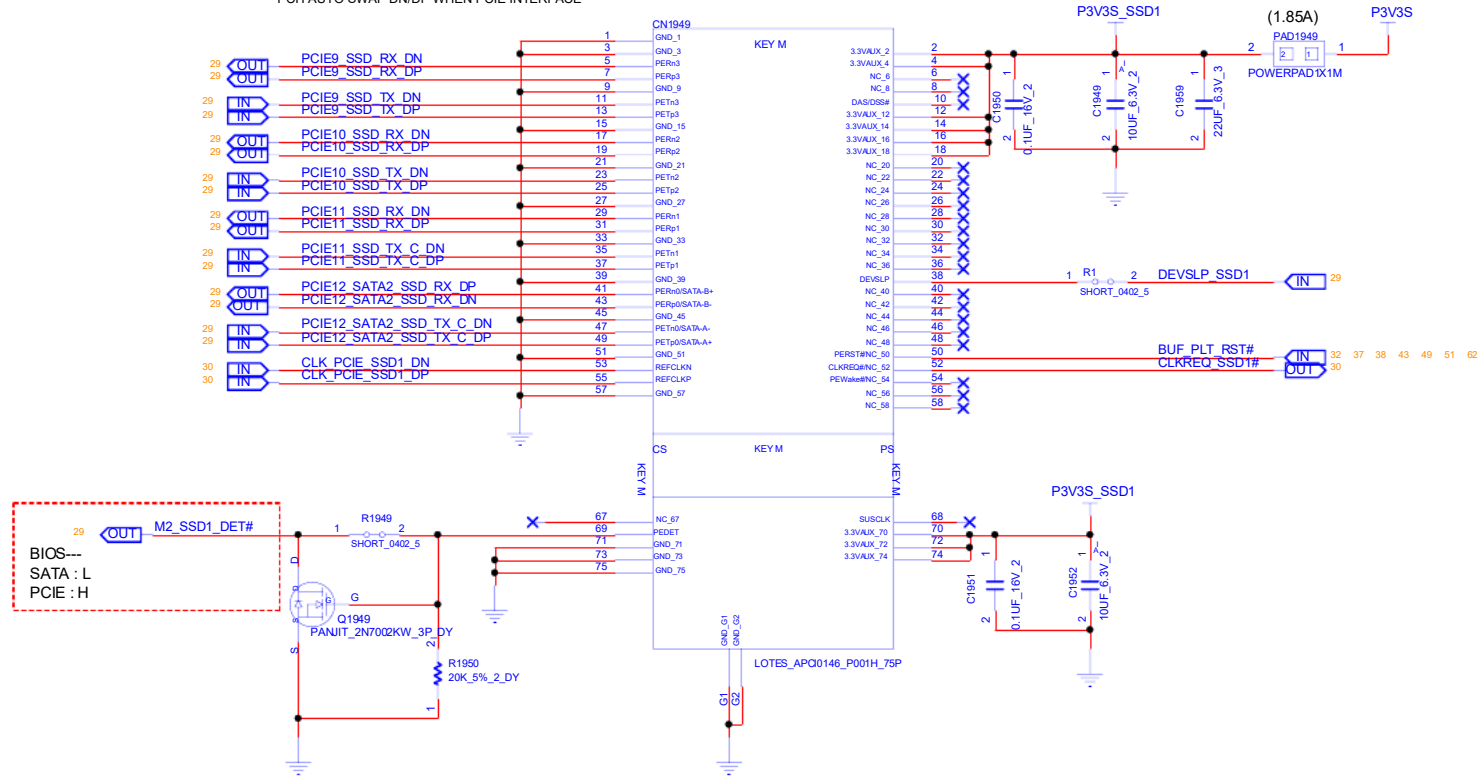
## INVENTEC

TITLE  
MODEL PROJECT:FUNCTION  
Block Diagram  
SIZE A3 CODE CS DOC NUMBER 1310A29944-0-0 REV X01  
SHEET 49 of 73

CHANGE by Loren Huang DATE 13-Dec.-2017  
PCB RN 605DA2994401 PCB VER X01

# NGFF SSD1(PCIE/SATA 4X)

PCH AUTO SWAP DN/DP WHEN PCIE INTERFACE



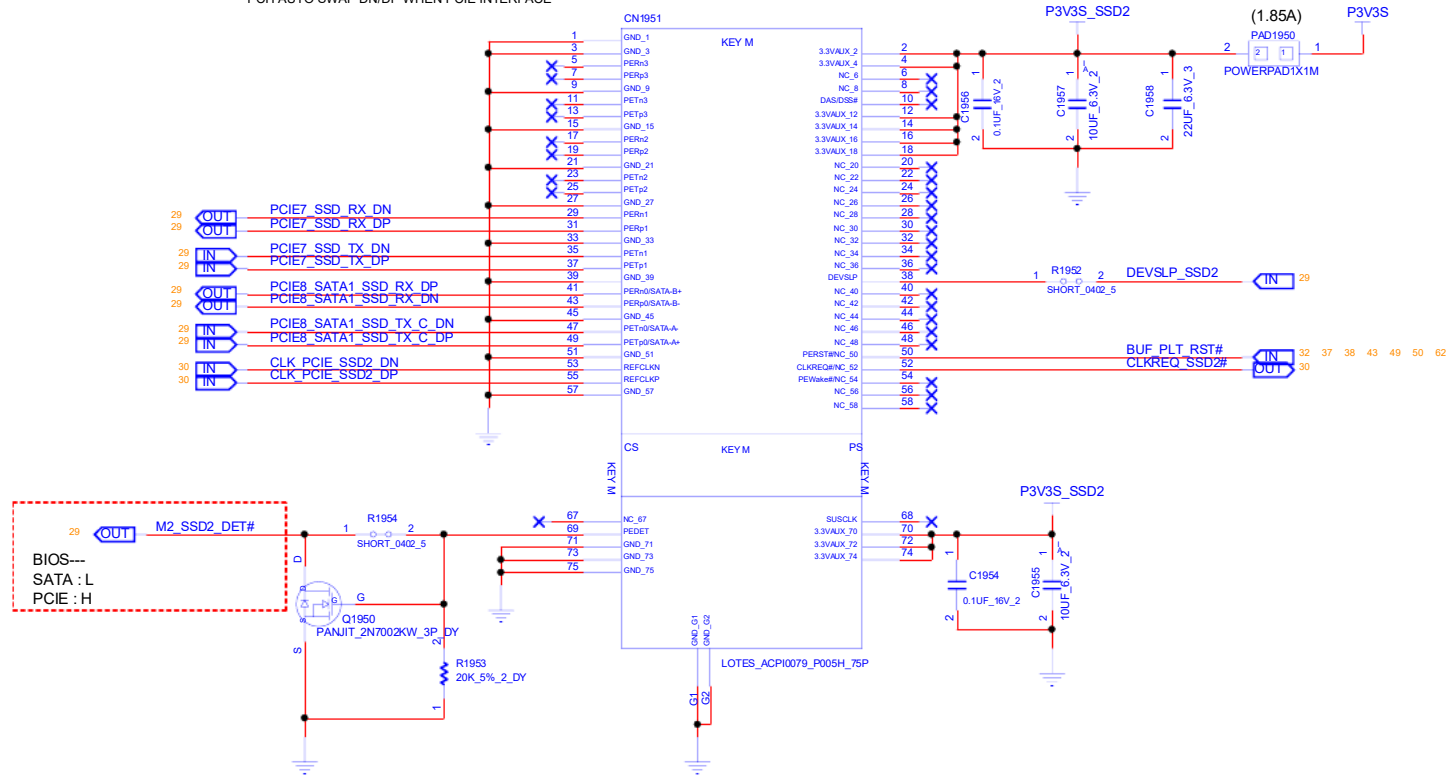
INVENTEC

TITLE			
MODEL PROJECT FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310A29944-0-0	X01
SHEET		50 of 73	

CHANGE by	Loren Huang	DATE	13-Dec-2017
PCB BN	6050A2994401	PCB VER	X01

# NGFF SSD2(PCIE/SATA 2X)

PCH AUTO SWAP DN/DP WHEN PCIE INTERFACE



M.2 CARD USES; SATA SIGNALING (LOW) OR PCIE SIGNALING (HIGH)

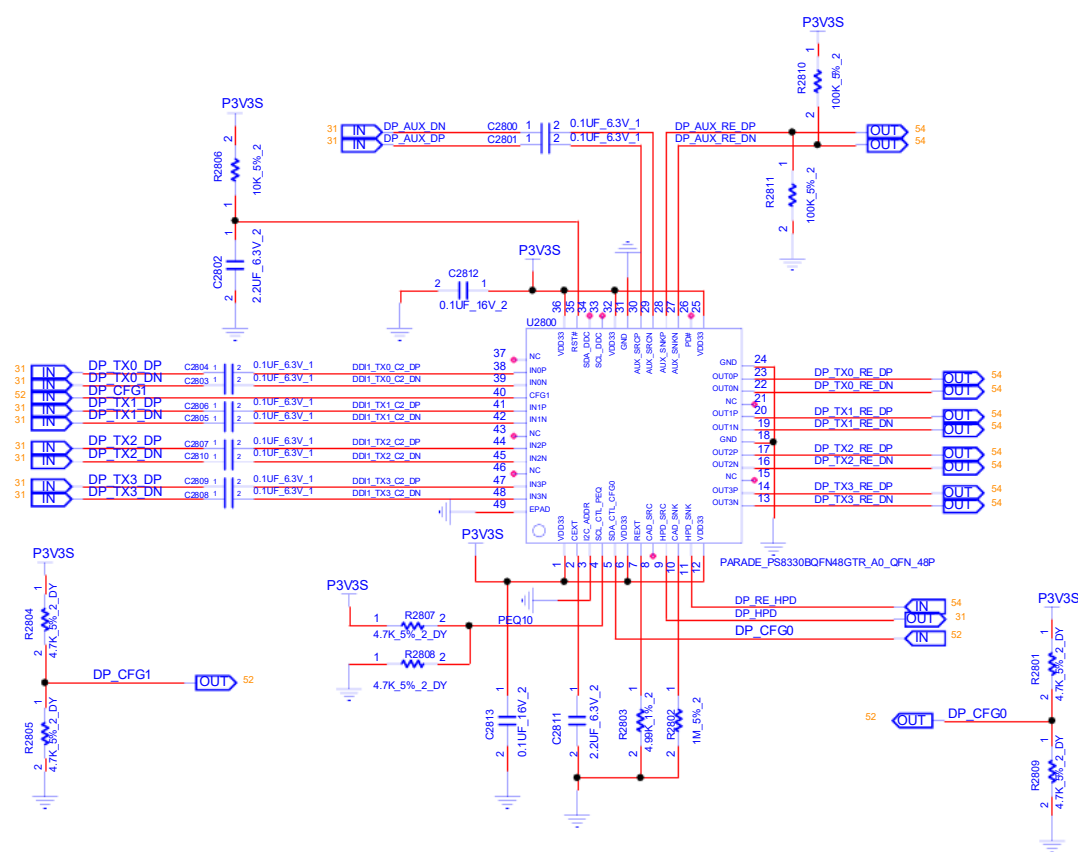
REFERENCE NUMBER:1950~1999

INVENTEC

TITLE			
MODEL PROJECT FUNCTION			
Block Diagram			
DOC NUMBER			
1310A29944-0-0			
REV			
X01			
SIZE	CODE	SHEET	
A3	CS	51 of 73	

CHANGE by	Loren Huang	DATE	13-Dec-2017
PCB PIN	6050A2994401	PCB VER	X01

# DP REDRIVER

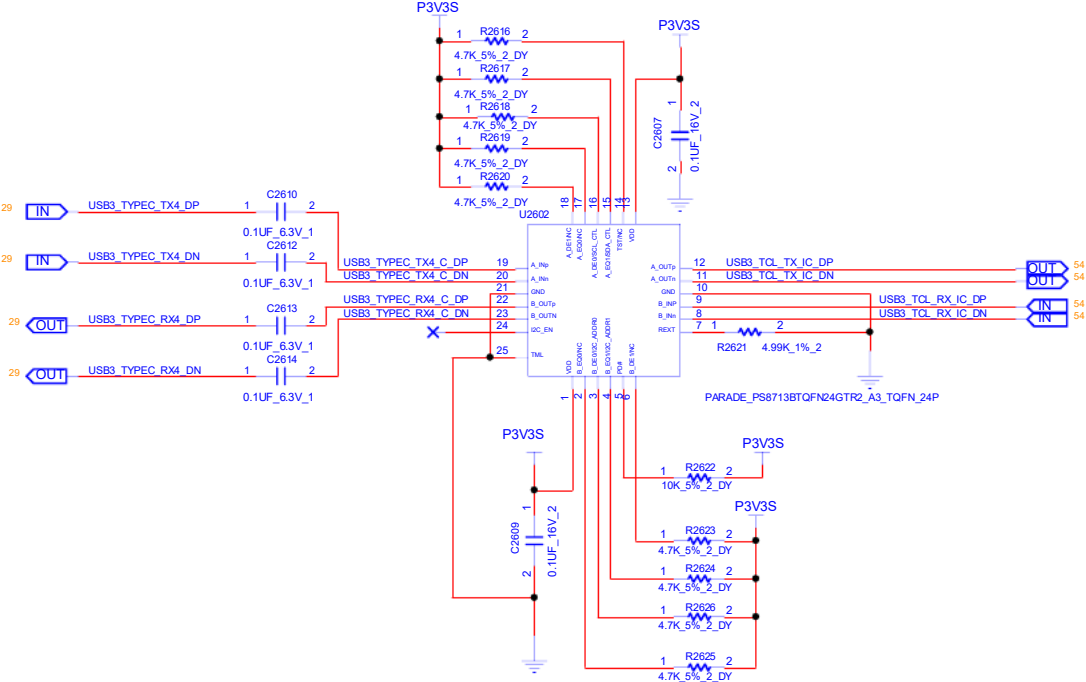


INVENTEC				
TITLE				
MODEL PROJECT.FUNCTION				
Block Diagram				
SIZE	CODE	DOCNUMBER	REV	
A3	CS	1310A29944-0-0	X01	
SHEET		82 of 73		

CHANGE by	Loren Huang	DATE	13-Dec.-2017
PCB PIN	6050A2994401	PCB VER	X01

# USB3 REDRIVER

REFERENCE 2600~2699(USB RESERVE)



INVENTEC

TITLE  
MODEL PROJECT FUNCTION  
Block Diagram

SIZE A3 CODE CS DOC NUMBER 1310A29944-0-0 REV X01

SHEET 83 of 73

CHANGE by Loren Huang DATE 13-Dec-2017  
PCB.DIN 6050A2994401 PCB.VER X01

	R2605	R2606
Slave Addr	Ra 1%	Rb 1%
addr0	NC	10K
addr1	54.9K	12.1K
addr2	27.4K	15.8K
addr3	18.2K	22.1K

Truth Table

SEL	OE	Y+	Y-
X	H	Hi-Z	Hi-Z
L	L	M+	M-
H	L	D+	D-

INVENTEC

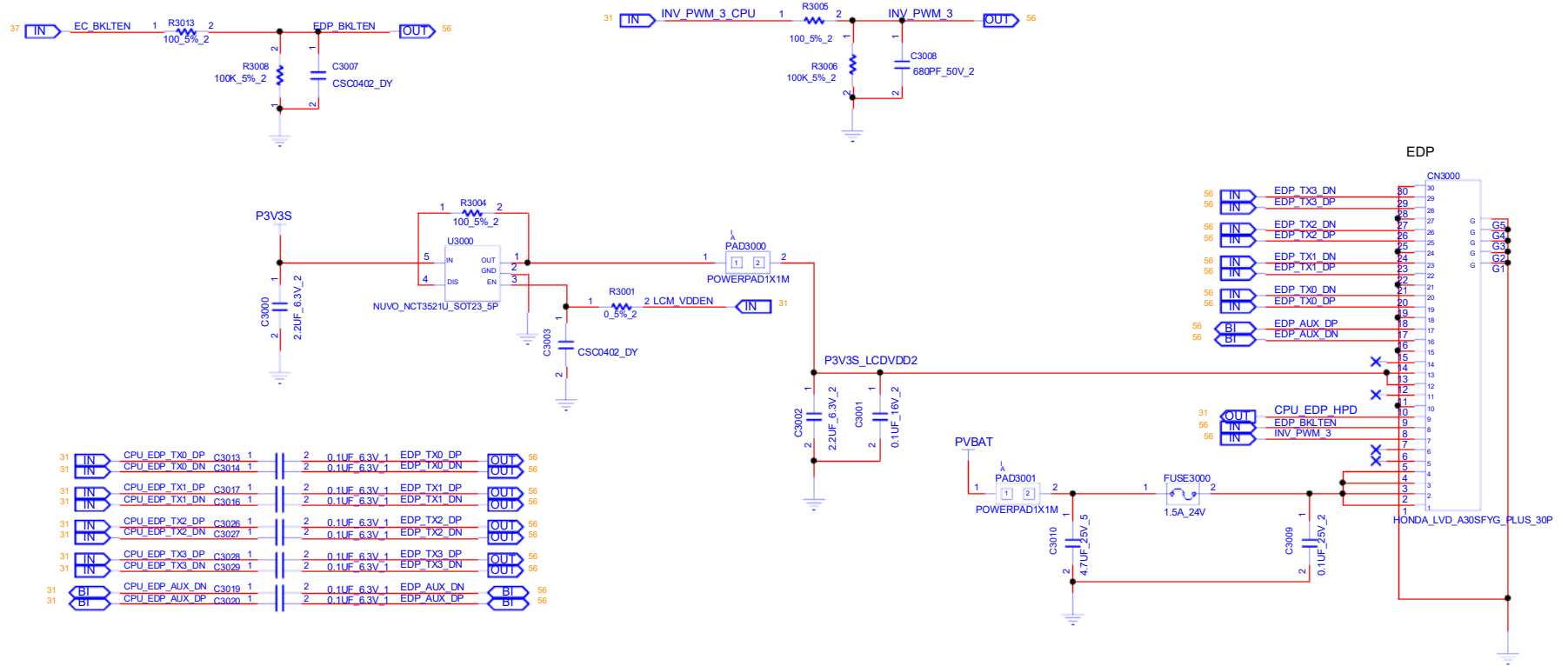
FILE	MODEL_PROJECT.FUNCTION
SIZE	TP95450
CODE	1310A29844-0
DOC NUMBER	
REV	X01

CHANGE BY	LYNN HUANG	DATE	13 Dec 2017
PCB P/N	6050A2094-01	PCB VER	X0002
SHEET	4	of 54	73



REFERENCE 3000-3049(LCM)

# EDP CONN



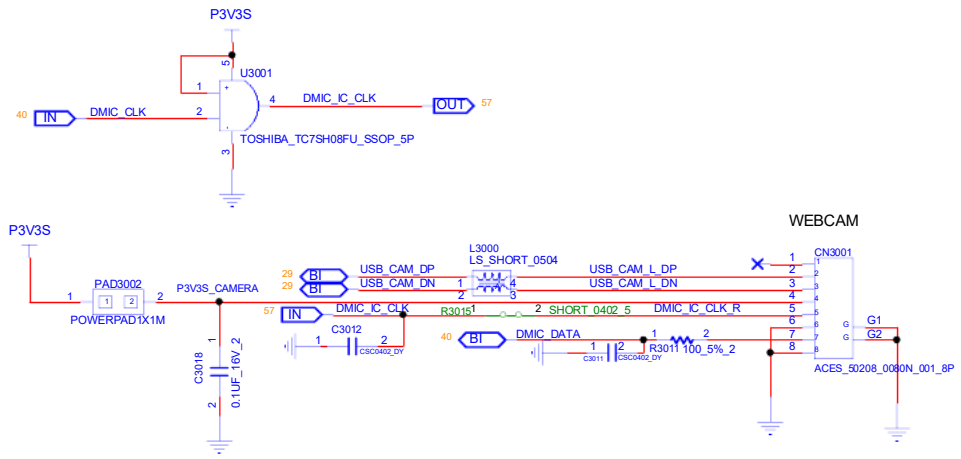
INVENTEC

TITLE  
MODEL PROJECT FUNCTION  
Block Diagram  
DOC NUMBER  
1310A29944-0-0  
REV  
X01  
SIZE  
A3  
CODE  
CS  
SHEET  
56 of 73

CHANGE by  
PCB.DIN  
Loren Huang  
6050A2994401  
DATE  
PCB.VER  
13-Dec-2017  
X01

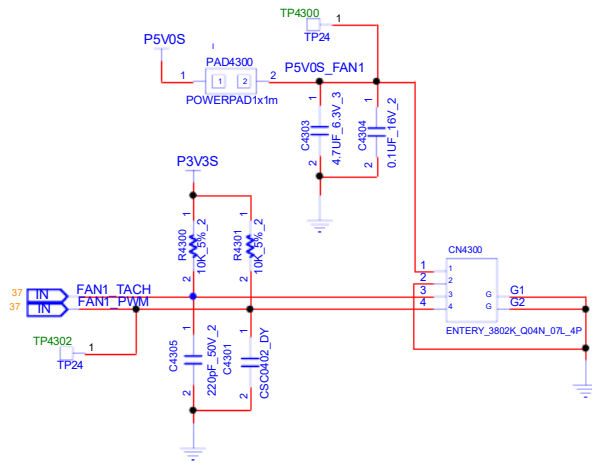


WEBCAM

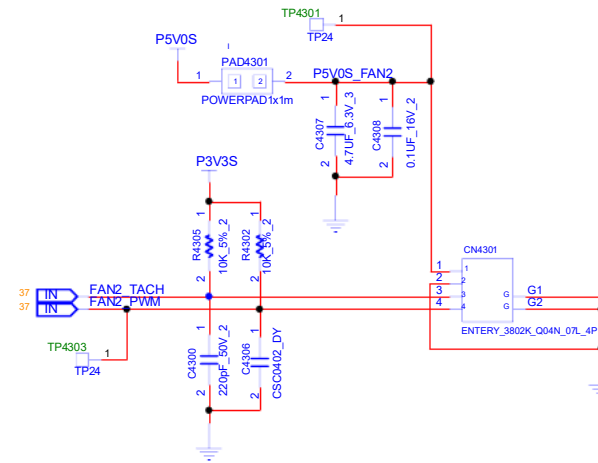


INVENTEC			
TITLE MODEL PROJECT FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310A29944-0-0	REV X01
CHANGE by PCB.DIN		DATE PCB.VER	13-Dec.-2017 X01
SHEET		87 of 73	1

REFERENCE 4300~4349(FAN)  
REFERENCE 4411~4449(THERMAL )



FAN1 CN CPU



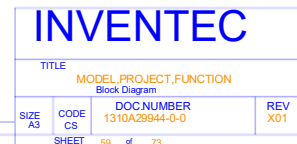
FAN2 CN CPU

REFERENCE NUMBER:4411~4449

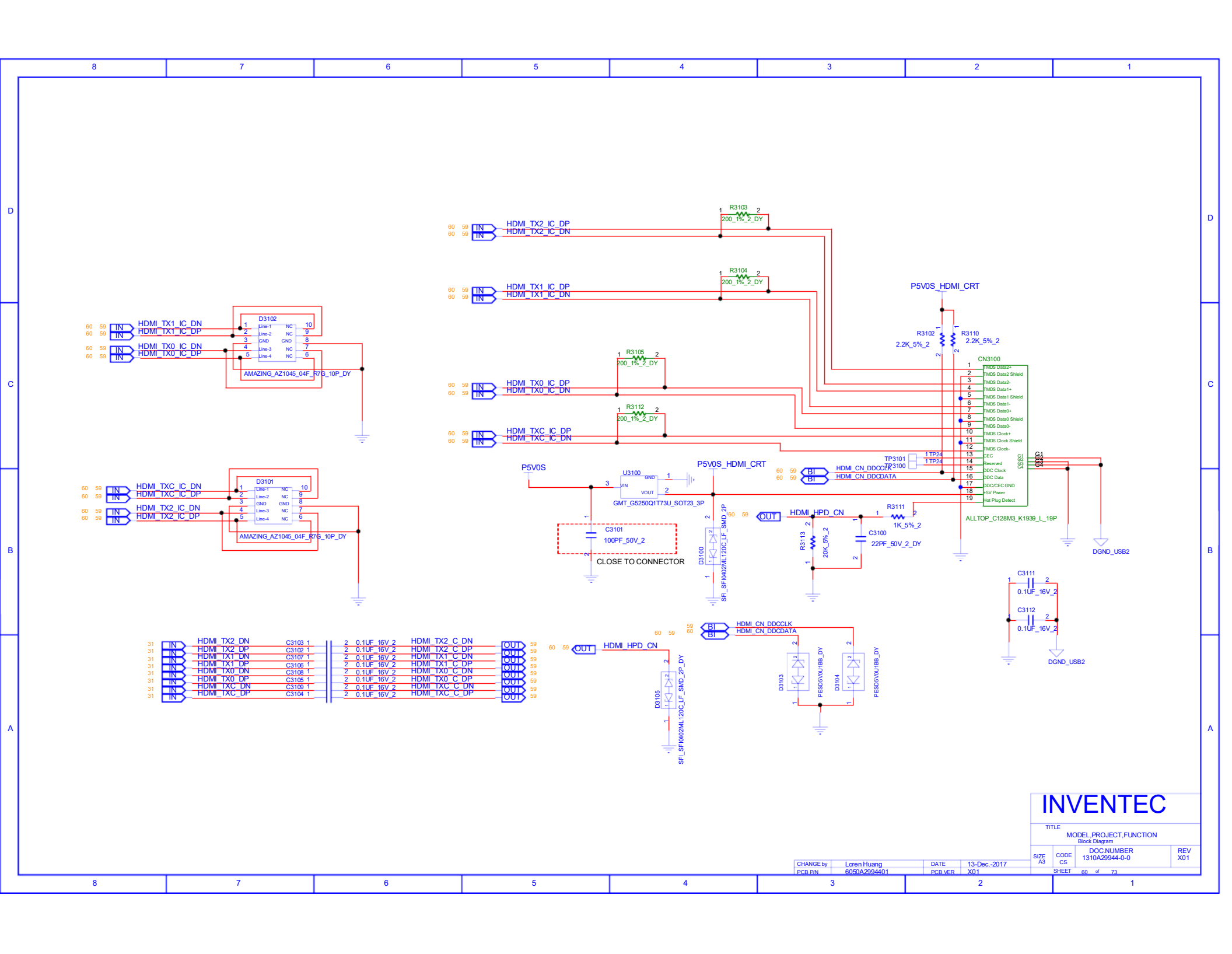
CHANGE by	Loren Huang	DATE	13 Dec 2017
PCB PIN	86N06-2994401	PCB VER	X13

INVENTEC			
TITLE			
MODEL PROJECT FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310A29944-0-0	X01
SHEET		of 58	73

# HDMI REPEATER (4K2K)



CHANGE by	Loren Huang	DATE	13-Dec.-2017
PCR P/N	6050A289/401	PCR VER	X01



INVENTEC

TITLE

MODEL PROJECT.FUNCTION

Block Diagram

DOC NUMBER

1310A29944-0-0

REV

X01

SIZE

A3

CODE

CS

SHEET

60 of 73

CHANGE by Loren Huang 6050A2994401 DATE 13-Dec.-2017 PCB VER X01

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NOTES:  
1.HSF Property:Comply iSupplier system HSF property attribute up-to-date value.

N17P G0 MAX-Q

GDDR5 29X29(4PCS)

2018.03.28

13 Dec -2017		
DATE	CHANGE NO	REV
		A

DESIGN DRAWER				DATE				13DEC-2017			
CHECK				AD1							
APPROVAL											
FILE NAME											
FOR P/B				DESIGN DRAWING				FOR M/R			
				2018							

Close to GPU

51 50 49 48 38 37 32

28

DGPU\_HOLD\_RST#

BUF\_PLT\_RST#

IN

IN

RS109

SHORT\_0402\_15

P1VB5\_AON1

1

2

1

2

C5348

0.1uF\_16V\_2

1.8V

62 66 72

PEG\_RST#

OUT

U5100

7C75208PU

RS115

100K\_5%\_2

C5301

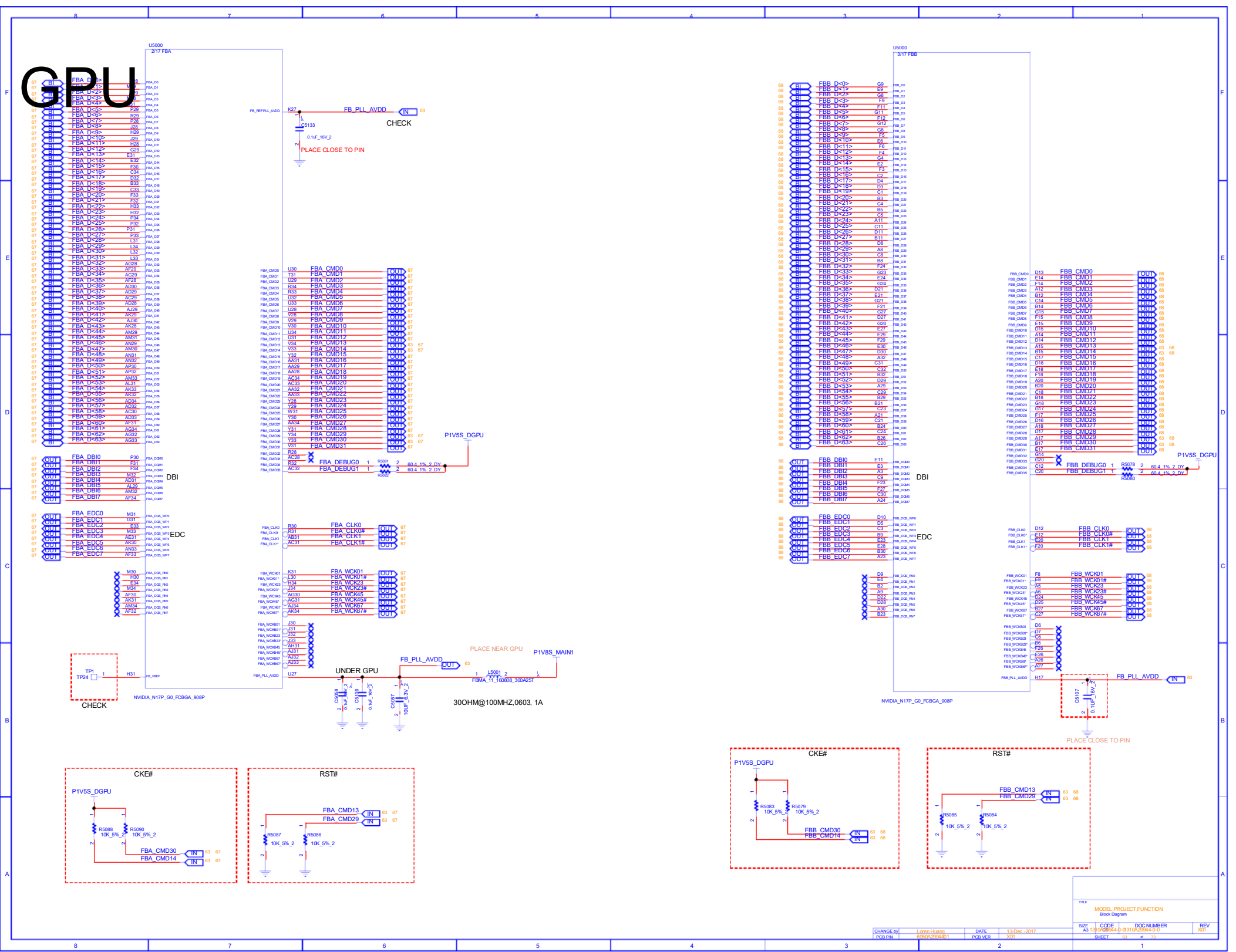
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RS404

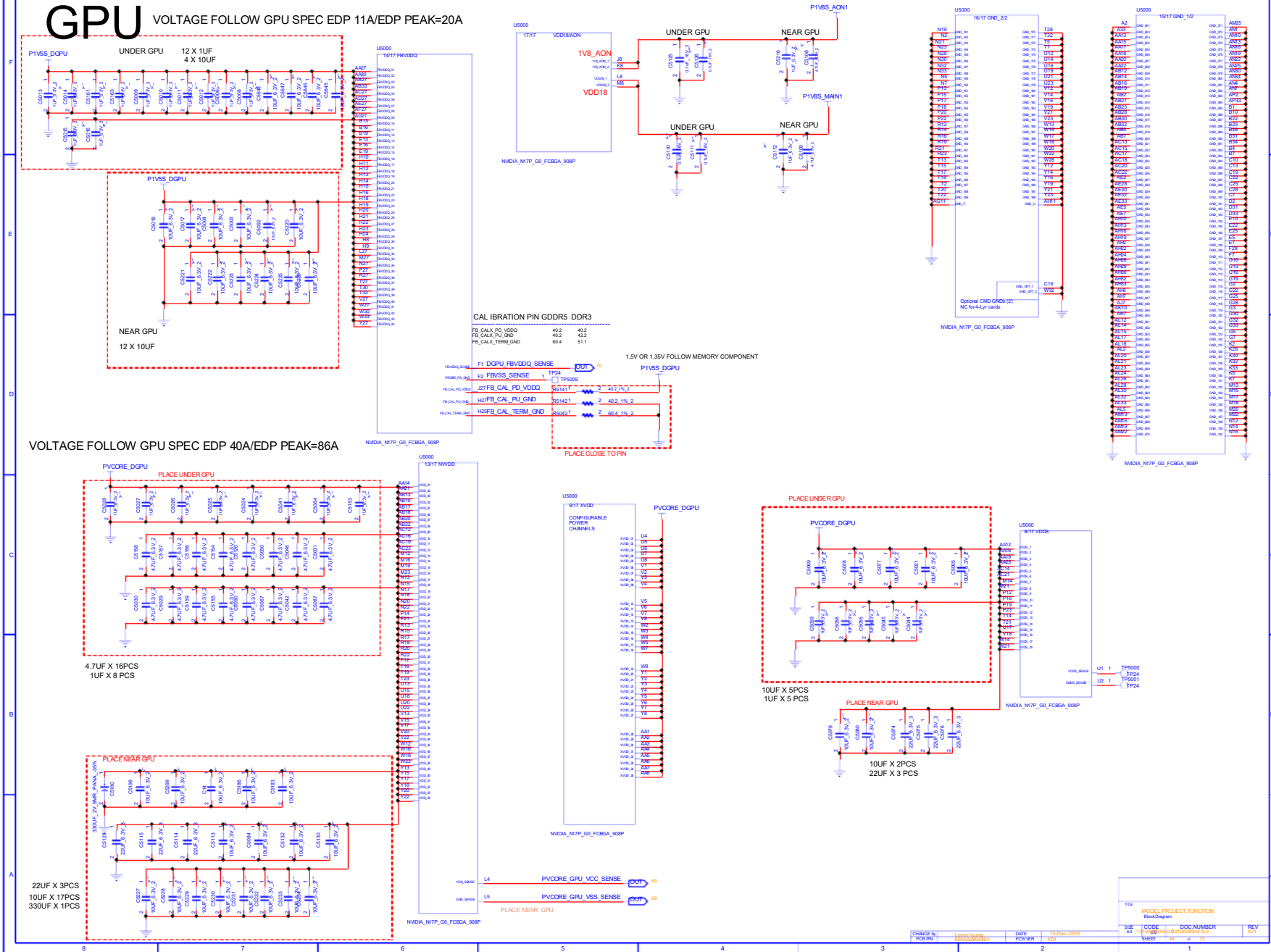
10K\_5%\_2



CHANGE by	Loren Huang	DATE	
PCB PIN	60599EN04-01	PCB VER	13-Dec-2017

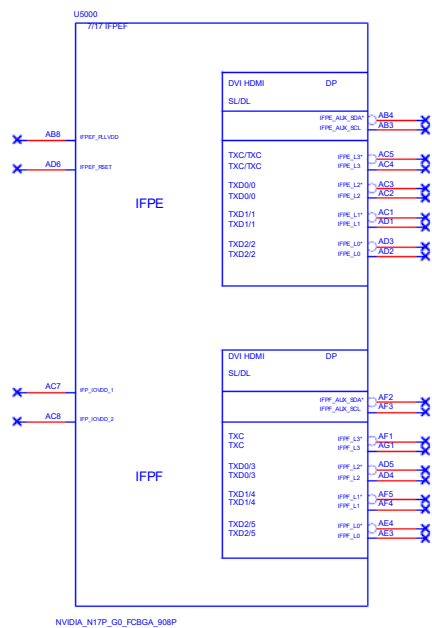
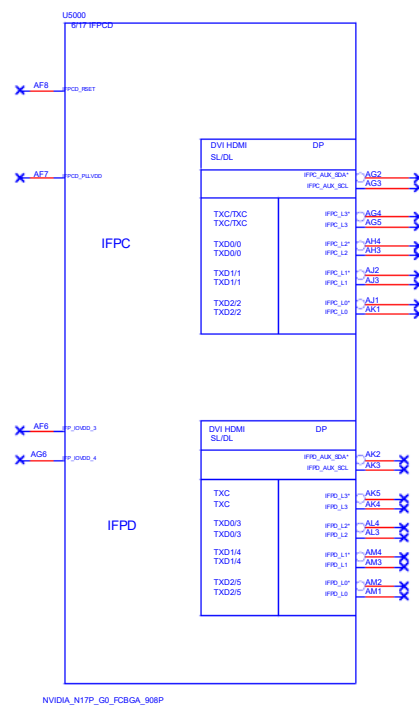
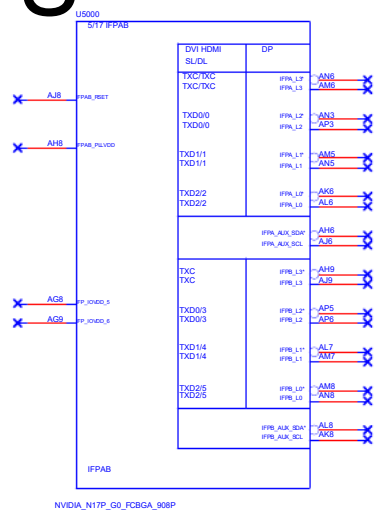


# GPU





## GPU



# GPU

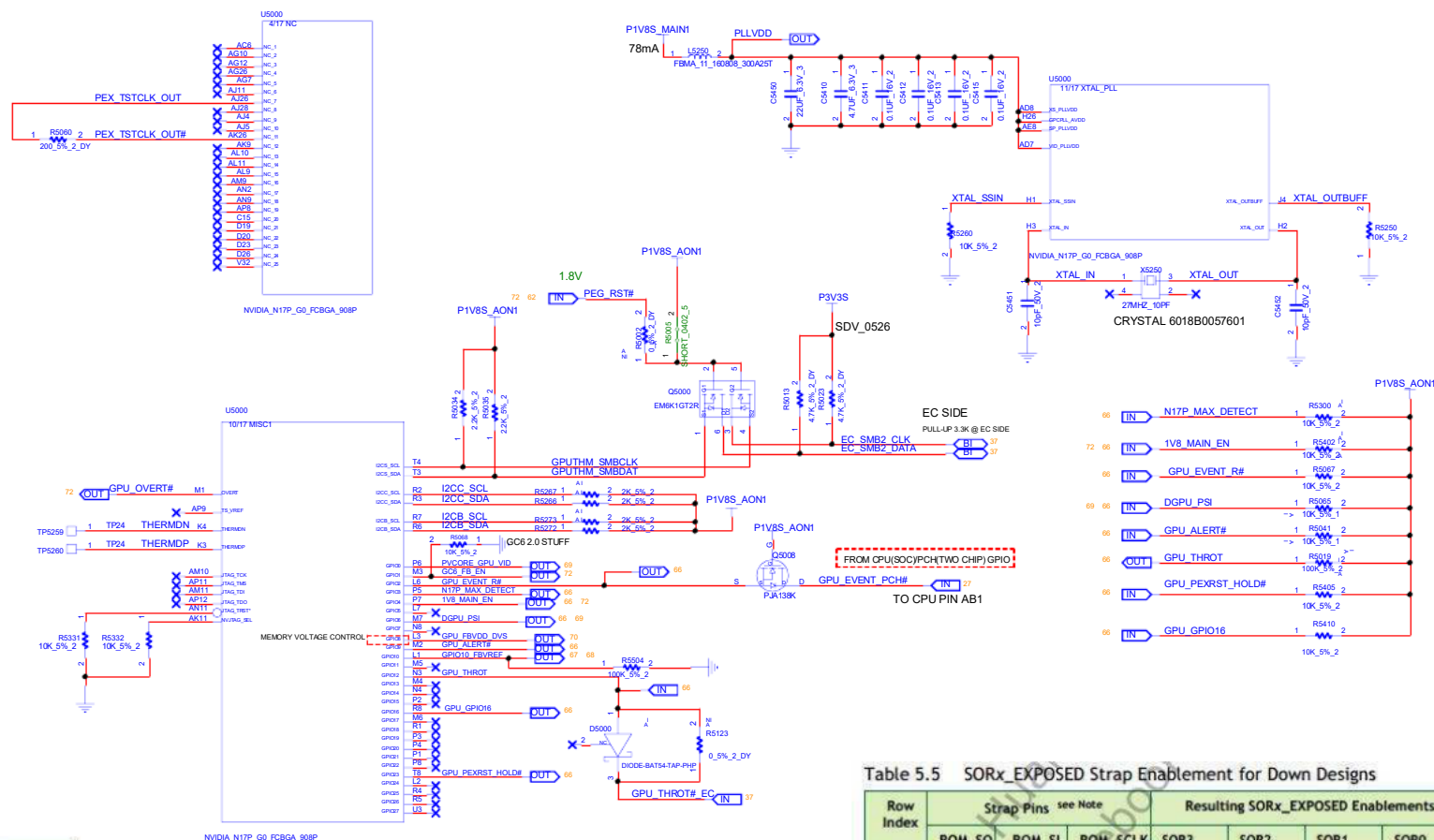


Table 5.3 RAMCFG

Strap Pins <small>see Note</small>			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)

Table 3. N17P-G0/-G1 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32	1.35V and 1.5V <sup>1</sup>	Samsung	K4G80325FB-HC28	B-die	0x0	7 Gbps	N/A	Full	Production ready
			Samsung	K4G80325FB-HC25	B-die	0x0	8 Gbps	N/A	N/A	Substitution allowed with waiver <sup>2</sup>
			Micron	MT51J256M32HF-70:A	A-die	0x1	7 Gbps	N/A	Full	Production ready
			Micron	MT51J256M32HF-80:A	A-die	0x1	8 Gbps	N/A	N/A	Substitution allowed with waiver <sup>2</sup>
			Hynix	H5GC8H24MUR-R0C	M-die	0x2	7 Gbps	N/A	Full	Post production ready
			Hynix	H5GQ8H24MUR-R4C	M-die	0x2	8 Gbps	N/A	N/A	Substitution allowed with waiver <sup>2</sup>

Table 5.6 SMB ALT\_ADDR, DEVID\_SEL, PCIE\_CFG, VGA\_DEVICE

Strap Pins <sup>Note 1</sup>			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVIC
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1

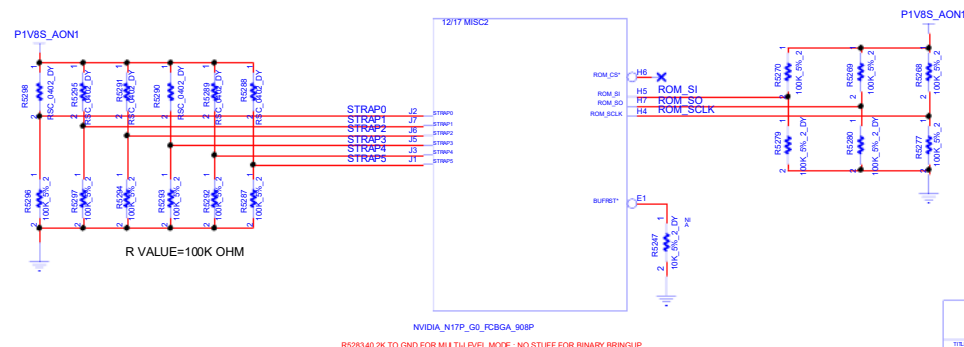


Table 5.5 SORx\_EXPOSED Strap Enablement for Down Designs

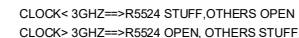
Row Index	Strap Pins <small>see Note</small>			Resulting SORx_EXPOSED Enablements			
	ROM_SO	ROM_SI	ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	H	ENABLED	ENABLED	ENABLED	disabled
13	L	H	L	ENABLED	ENABLED	disabled	ENABLED
12	L	H	H	ENABLED	ENABLED	disabled	disabled
8	H	H	H	ENABLED	disabled	disabled	disabled
0	H	H	M	disabled	disabled	disabled	disabled
	M	X	X	(Reserved; do not configure)			
	All other Strap Configurations			(Reserved)			

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# GDDR5 CHANNEL A



P1V5S DGPL



10\*1UF

INVENTEC

MODEL, PROJECT, FUNCTION		
Block Diagram		
SIZE C	CODE CS	DOC NUMBER 1310A29944-0-0
SHEET		of 67 7

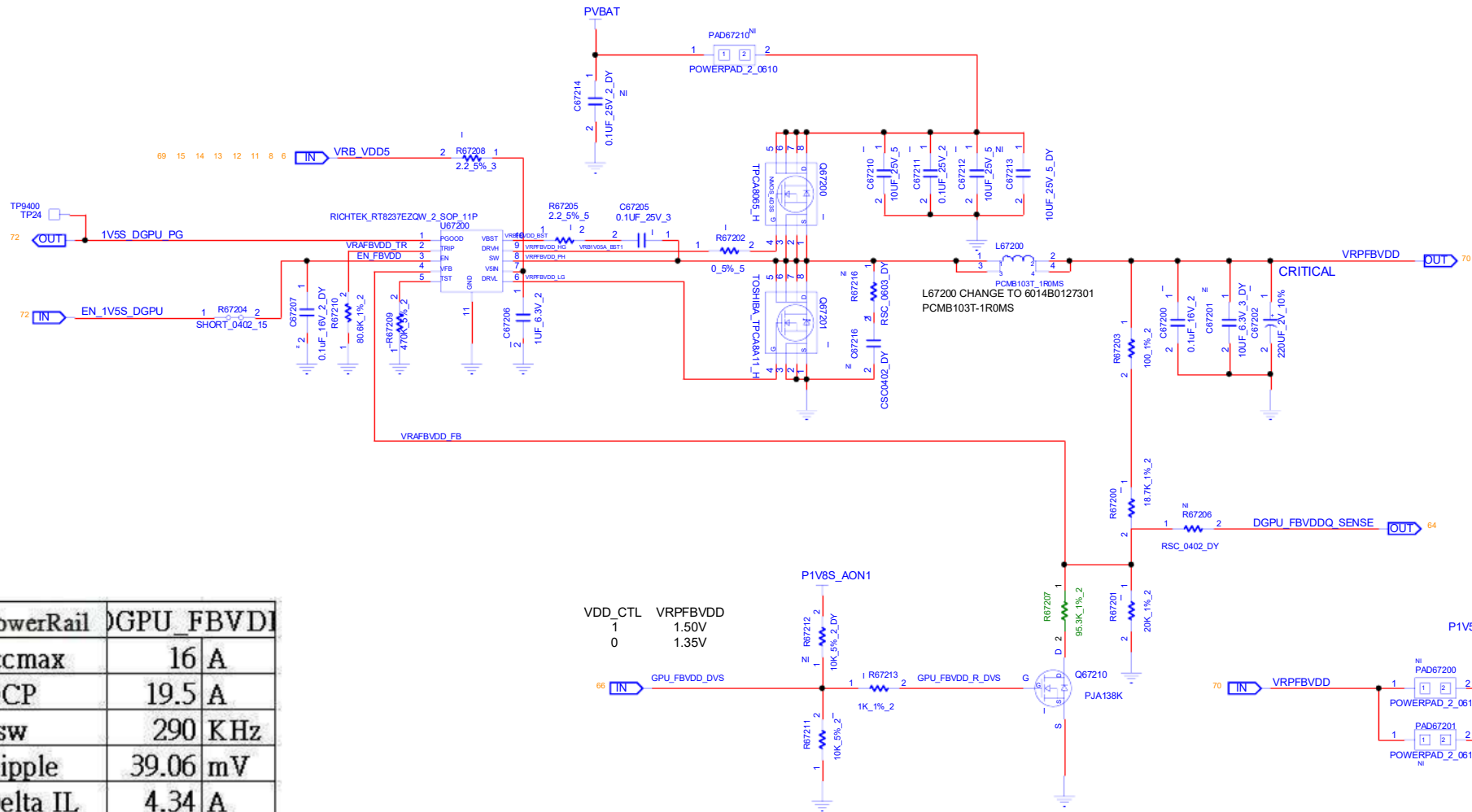
# GDDR5 CHANNEL B



SIZE C	CODE CS	DOC. NUMBER 1310A29944-0-0
SHEET		of 68



# DGPU-FBVDD

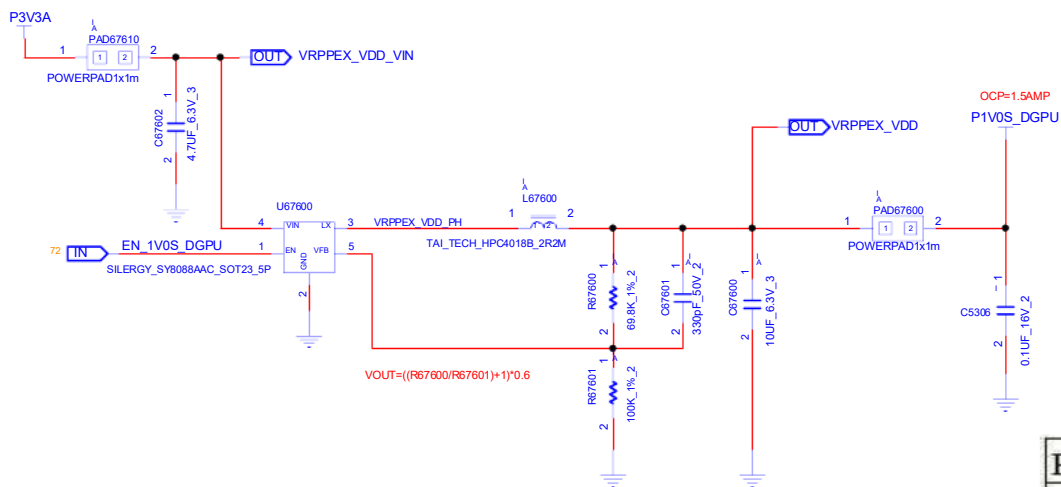


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TITLE  
MODEL PROJECT FUNCTION  
Block Diagram  
DOC NUMBER  
1310A29944-0-0  
REV  
X01

CHANGE by  
Loren Huang  
6050A29944-01  
DATE  
13-Dec-2017  
PCB VER  
X01

SIZE  
A3  
CODE  
CS  
SHEET  
70 of 73



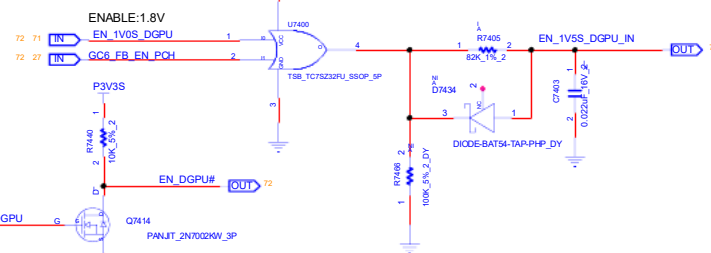
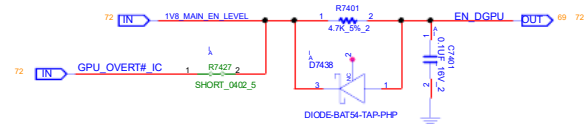
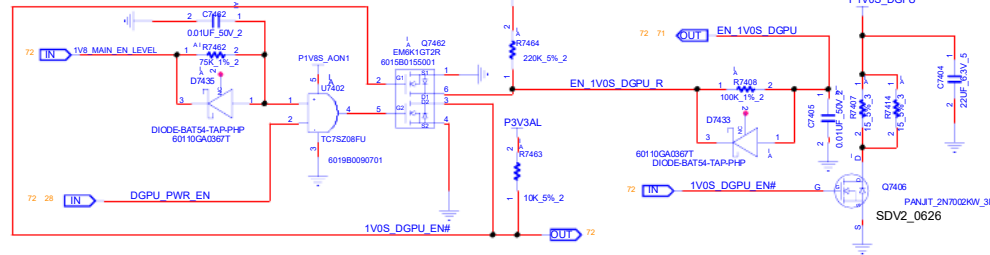
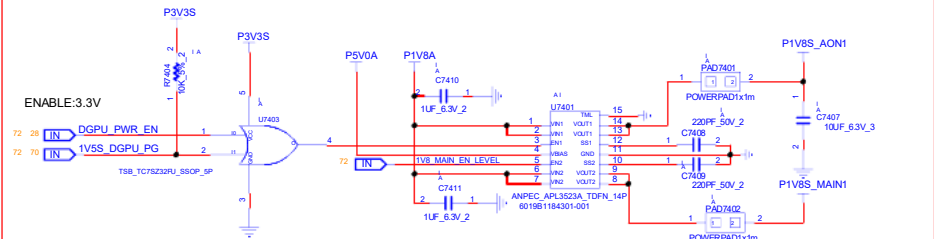
PowerRail	PEX_VDD	
Iccmax	1.1	A
OCP	1.6	A
Fsw	1500	KHz
Ripple	3.49	mV
Delta IL	0.53	A

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TITLE  
MODEL PROJECT FUNCTION  
Block Diagram

SIZE A3 CODE CS DOC NUMBER 1310A29944-0-0 REV X01  
SHEET 71 of 73

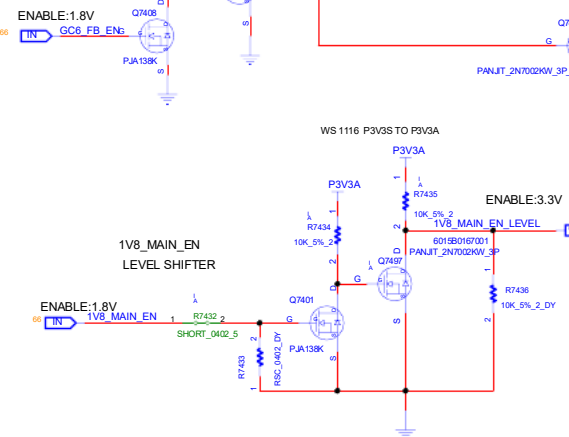
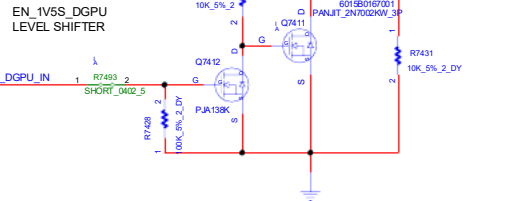
CHANGE by Loren Huang DATE 13-Dec-2017  
PCB.DIN 6050A2994401 PCB.VER X01



FOR GC6 2.0

DISCHARGE

DISCHARGE

EN\_1V5S\_DGPU  
LEVEL SHIFTER

PEG\_RST#  
LEVEL SHIFTER

ENABLE:1.8V

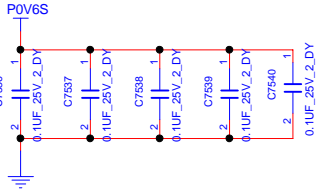
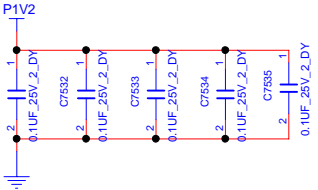
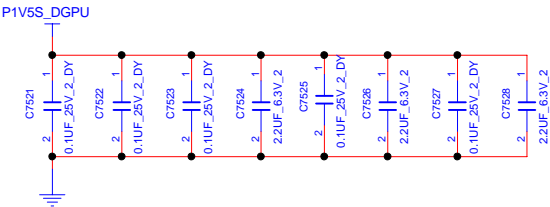
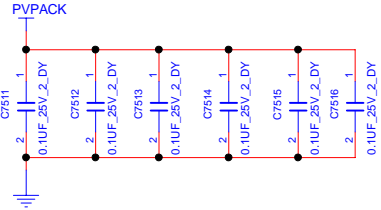
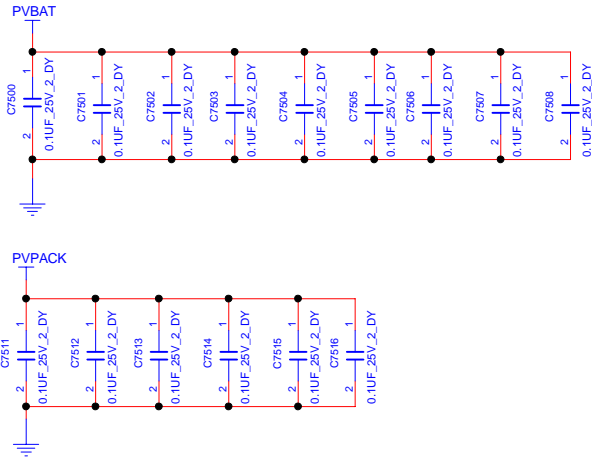
## INVENTEC

TITLE MODEL,PROJECT,FUNCTION  
Block Diagram

CHANGE by	Loren Huang	DATE	13-Dec.-2017	SIZE A3	CODE CS	DOC NUMBER 1310A29944-0-0	REV X01
PCB.PIN	6060A2994401	PCB VER	X01	SHEET 72 of 73			



RF&EMI



INVENTEC				
TITLE				
MODEL PROJECT,FUNCTION Block Diagram				
SIZE A3	CODE CS	DOC NUMBER 1310A29944-0-0		REV X01
CHANGE by PCB P/N		DATE PCB VER		SHEET 73 of 73

CHANGE by	Loren Huang	DATE	13-Dec-2017
PCB P/N	6050A2994401	PCB VER	X01